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DIGITAL SYNTHESIZER AND CODE GENERATOR.(U)

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DIGITAL SYNTHESIZER AND CODE GENERATOR

RCA
Advanced Technology Laboratories
Government and Commercial Systems
RCA
Camden, New Jersey 08102

JUNE 1976

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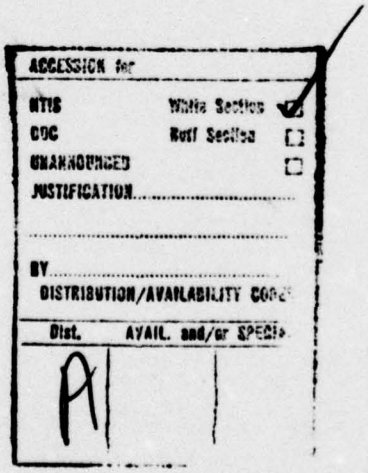

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The objective of this program was to design, fabricate, and test two building block modules for application to digital modems. The two modules selected for implementation were a digital code generator operating to 20 Mb/s and a digital synthesizer providing a 25-kHz bandwidth centered at 200 kHz, with a frequency

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Block 20 (cont.)

resolution of 4 Hz. Both the code generator and frequency synthesizer modules were implemented using the silicon-gate CMOS/SOS technology.

The code generator array contains a 16-stage sequence generator capable of being operated with various code lengths from 1 to 16 stages. The code generator operates at 20 Mb/s output rates at 10 V with approximately 105 mW of power dissipation. At 5 V the generator operates at 10 Mb/s with 10 mW of dissipation.

The digital synthesizer LSI array that was designed under this program is coupled to a phase-locked loop and output bandpass filter to form the synthesizer module. Mounted on a 4.5 inch by 8.5 inch printed circuit card, the synthesizer module provides for the generation of 419,430 frequencies over the 25-kHz band of interest. The frequency resolution of the delivered synthesizer is 0.0596 Hz, compared to the Government's original requirement for resolution of 4 Hz.

FOREWORD

The work reported in this Technical Report was performed under Air Force Contract F33615-74-C-1123, entitled, "Digital Synthesizer and Code Generator," by the RCA Advanced Technology Laboratories (ATL) and the Government Communication Systems Division (GCSD) of Government and Commercial Systems, Camden, N.J., and by the Solid State Technology Center (SSTC), Somerville, N.J.

This work was monitored by the Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio; Mr. Robert M. Werner (AFAL/DHE) was Project Engineer.

The following RCA personnel contributed to the work and to this report: H.W. Kaiser (Project Leader), W.F. Gehweiler (Project Engineer), J.I. Pridgen, and W.E. Arrowood. The LSI arrays were processed under the direction of H. Borkan of SSTC and were tested by W.F. Zlupko of ATL.

This final program report covers work performed from 15 June 1974 to 30 December 1975.

This report was released by the authors 27 February 1976.

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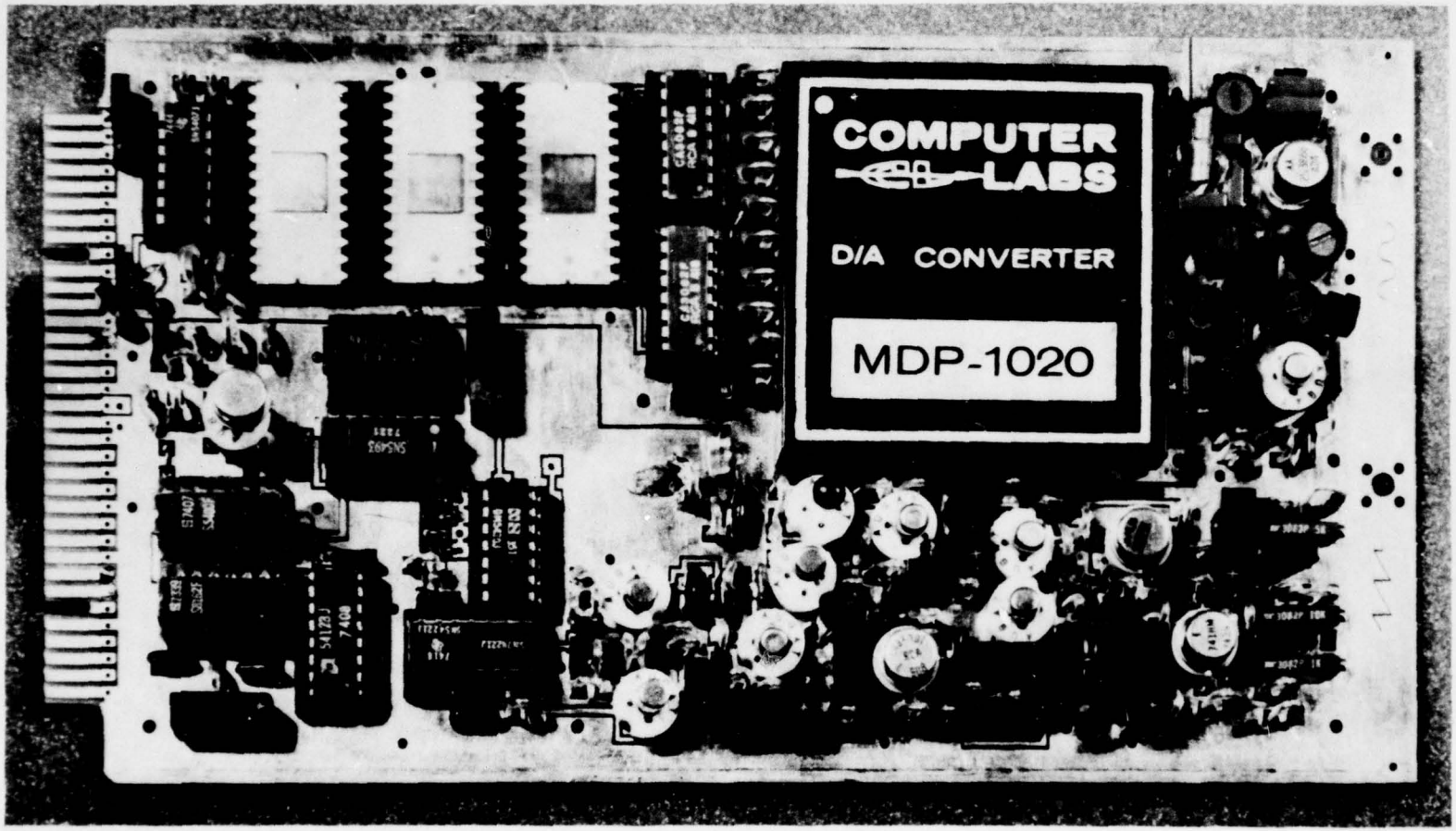


Frontispiece. Digital synthesizer module.

Section I

INTRODUCTION

This program is an advanced development effort to provide the Air Force with two digital communication system building block modules.

The first of these modules to be described in this report is a universal 16-stage code generator. The basic generator stage is a shift register and modulo-2 adder coupled together. The second input to the modulo-2 adder can be programmed to connect to a fixed voltage or to the output code sequence. This internal programmability feature allows many different code lengths and sequences to be generated. Additional programmable features allow for storage of two different code parameters internally to the chip so that the generator can be instantly switched from one code sequence to the other by one dc control lead.

Other system design features, as well as performance of the array, are discussed in the following sections of this report.

Following the technical discussion on the code generator, the second building block module is discussed, namely, an arithmetic synthesizer that provides for the generation of 419,430 frequencies over a 25-kHz bandwidth centered at 200 kHz.

Two different implementations of the basic arithmetic synthesizer have been fabricated and tested, and the results are provided in later sections of this report. The CMOS/SOS LSI synthesizer array that has been designed, fabricated, and tested and forms the heart of the synthesizer module, is also described in detail. Testing of the synthesizer module and application to several systems have suggested some design modifications that could be made to improve overall performance. These considerations are also discussed.

This program started in June 1974 and ended in December 1975.

Section II

REPORT SUMMARY

A. PROGRAM OBJECTIVES

The objective of this program was to design, fabricate, and test two building block modules for application to digital modems. The design objectives were to incorporate sufficient universal design features to provide off-the-shelf hardware that would result in cost-effective implementation of data communication modems.

The two modules selected for implementation by this program were a digital code generator operating to 20 Mb/s and a digital synthesizer providing a 25-kHz bandwidth centered at 200 kHz, with a frequency resolution of 4 Hz.

Primary consideration has been given to the application of LSI design techniques to both of the selected building blocks.

B. PROGRAM RESULTS

Both the code generator and frequency synthesizer modules have been successfully implemented using the silicon-gate CMOS/SOS technology. In achieving the program objectives, two LSI array types have been designed, fabricated and tested, namely, a 16-stage universal code generator and an 8-stage arithmetic synthesizer. The technical objectives of the program have been met, and in many cases greatly exceeded, as demonstrated by the performance of the units. For instance, a frequency synthesizer with greater resolution and much faster hopping rates has been demonstrated. A summary of these design parameters follows.

C. CODE GENERATOR ARRAY (TCS045)

An LSI CMOS/SOS code generator array that completely satisfies the original code generator module requirements has been designed and successfully tested. Although this design is based on the Government specifications, it is amended with features derived from RCA system experience. The resulting code generator array, TCS045, contains a 16-stage sequence generator capable of being operated with various code lengths from 1 to 16 stages. The code generator operates at 20 Mb/s output rates at 10 V with approximately 105 mW of power dissipation. At 5 V the generator operates at 10 Mb/s with 10 mW of dissipation.

Additional features incorporated into the array allow two different codes to be generated on the basis of data stored in memory located on the array. The code generator can be reset to a given state defined by a 16-bit word serially stored in another on-chip memory offering a capability to update code sequences for time-of-day information, for example. A high-speed register allows the readout at a rate up to 50 Mb/s of the state of the generator at a particular time. The parallel-to-serial conversion is accomplished on-chip.

The code generator is packaged in a 28-lead dual in-line ceramic package. Thirty arrays were delivered to AFAL.

D. DIGITAL SYNTHESIZER MODULE

The synthesizer system design requirements have been met by the design of an arithmetic synthesizer coupled to a phase-locked loop and output bandpass filter. The module is contained on a 4.5 inch x 8.5 inch printed circuit card (see Frontispiece) and provides for the generation of 419,430 frequencies over the 25-kHz band of interest. The frequency resolution of the delivered synthesizer is 0.0596 Hz, compared to the Government's original requirement for resolution of 4 Hz.

The spurious output frequencies are on the average better than 70 dB below the center frequency, with the noise floor of the output more than 90 dB down. The worst-case spurious signal observed was better than 55 dB down from the center frequency. For certain synchronous frequencies, where the product of the clock sampling frequency and the input word size is an integral submultiple of the accumulator size, the performance of the synthesizer is greatly improved by the virtual elimination of all spurious signals.

The worst case settling time of the synthesizer has been shown to be 75 μs for a 25-kHz jump, compared to the design goal of 300 μs.

The synthesizer module design is based on the use of a CMOS/SOS building block arithmetic synthesizer array (TCS047) and uses three of these arrays to implement the complete function.

A system utilization survey identified a 32-stage arithmetic synthesizer as representing the maximum size required for a broad range of applications and thus, served as a baseline design consideration. An 8-stage partition of the arithmetic synthesizers resulted from the design effort, and three of these arrays were incorporated into the synthesizer module to provide 24 stages resulting in the previously mentioned frequency resolution.

The synthesizer array can operate at clocking rates up to 19 MHz at 10 V with greater than 20 MHz performance at 12 V.

Five synthesizer modules containing 15 TCS047 arrays were delivered to the Air Force. In addition, 15 synthesizer arrays were delivered separately.

The primary design emphasis was placed on the development of a synthesizer module operating with a sawtooth waveform from the synthesizer arrays. Of the five modules delivered, four modules were of this configuration. The fifth module was modified to test the performance characteristics of the synthesizer operating with a triangular waveform from the synthesizer and without the phase-locked loop. Although the spurious signal level was about 10 dB worse than the original configuration, the reduced parts count and relative simplicity of the synthesizer warrant its consideration for specific applications not requring the higher spectral purity.

E. REPORT CONTENTS

Section III.A contains a description of the TCS045 code generator, theory of operation, design implementation and test results obtained on 30 arrays. Recommendations for further design enhancements are also included in this section. Engineering specifications that serve as the baseline for a production specification have been derived; the specifications are based on an analysis of the test results and computer simulations for the code generator.

Section III.B describes the frequency synthesizer module. An overview of the operation of arithmetic synthesizers is presented in III.B.1. Detailed design information for the development of the associated CMOS/SOS synthesizer arrays (TCS047) is given in Section III.C.2, along with theory of operation, logical implementation of the array and test results of 30 arrays. Engineering specifications are given for the TCS047 array, as well as several recommendations for design improvements.

Section III.D describes the incorporation of three synthesizer arrays with a phase-locked locked loop and output filter to provide for the specified 200 kHz center-frequency synthesizer. A description of the operation of the phase-locked loop in conjuction with the sawtooth output of the synthesizer array is provided, along with a description and performance characteristics of the output filter. Although the primary design emphasis was centered on the sawtooth operation type of synthesizer, testing of a triangular waveform synthesizer without a phase-locked loop was also accomplished on this program and is reported in Section III.D.2.c. To gain perspective on the performance characteristics of arithmetic synthesizers, many spectrum plots have been included, covering a wide range of frequency select words, clocking frequencies and output frequencies. Curves have been included for both the sawtooth synthesizers as well as the triangular waveform synthesizer. Several design modifications suggested for the module circuitry are also presented in Section III.D.2.f. A reliability prediction made for the synthesizer module is given in Section III.E.

Appendix A contains the design details of the phase-locked loop bandpass and lowpass filters. Appendix B contains setup and alignment procedures for the synthesizer module, and Appendix C provides a simple hand-held calculator algorithm for determining the digital value of the input frequency select word for given sampling clock and output frequencies.

F. CONCLUSIONS

The CMOS/SOS technology has been shown to be an effective LSI technology for implementation of communication building blocks. The complete requirements for the code generator module have been met by a single LSI array that operates at the required frequency of 20 Mb/s while dissipating only 105 mW. A significant reduction in power dissipation to 10 mW is possible for operation at 10 Mb/s.

The code generator design has proven to be sufficiently flexible in system utilization capability that it has been incorporated in demonstration equipment and proposed for use in several Government systems. As a result of system application, several design improvements have been proposed as described elsewhere in this report.

The CMOS/SOS arithmetic synthesizer LSI array has also proved to be an effective synthesizer building block. The 8-bit slice partitioning of the overall logic for an arithmetic synthesizer allows various size and performance synthesizers to be fabricated to suit a particular requirement. Sufficient flexibility has been provided to meet most complex requirements for near future equipments. For example, by using a 1-MHz sampling clock and a 32-stage arithmetic synthesizer, a frequency resolution of 0.000233 Hz can be achieved.

Standard production design rules and processes have been used in the fabrication of the code generator and synthesizer arrays. These processes were developed as part of the Air Force Materials Laboratory contract F33615-73-C-5043 with RCA Solid State Technology Center.

A significant understanding of the general performance factors associated with arithmetic synthesizers was obtained during this program. A basic knowledge of these factors is essential before the synthesizers can be applied to a system. Generally speaking, the arithmetic synthesizer is an efficient and cost-effective method of frequency generation. However, where a high degree of spectrum purity is important, additional circuits may be required to satisfactorily implement the system.

A triangular waveform arithmetic synthesizer will generally provide a spurious signal level 30 to 40 dB below the center frequency. a sawtooth synthesizer alone will be about 10 dB worse. The use of a phase-locked loop as developed for this

program will add about 40 to 50 dB of additional attenuation for the spurs. For frequency bandwidth greater than an octave, a sine lookup ROM should be considered to convert either the sawtooth or triangular waveforms to a sine wave. Such a conversion would eliminate the lower-order harmonics that could fall in the passband of the output filter for a broadband system.

The test and evaluation of the synthesizer array and associated module circuitry resulted in several proposals for design enhancements. These are described in the following sections of this report.

Section III

TECHNICAL DISCUSSION

A. CODE GENERATOR

1. General Operation

The code generator, TCS045, is a universal pseudorandom sequence generator with programmable feedback taps contained on a single custom-designed CMOS/SOS LSI array. The array configuration was chosen for maximum versatility in using the code generator for diverse applications.

The primary functional units of the code generator are shown in Figure 1. The pseudorandom sequence is produced in a 16-stage PRN generator by feeding the output back to exclusive-OR gates located between successive code-generator register stages. The particular sequence being generated is determined by the selection of stages to receive the feedback. The stages receiving the feedback are specified by one of two integral 16-bit memories, the acquire mode memory and the track mode memory. Thus, the feedback tap information for two different codes are stored in the array, one which may be used to acquire a signal and the other for tracking the signal in a particular application. The code generator is easily switched back and forth between the two modes.

Three additional 16-bit serial registers are provided to increase the versatility of the code generator array. The first of these, the control mode input register of Figure 1, is used to enter the feedback tap specification words into the two memory registers. Hence, any feedback tap combination can be programmed into the array.

The vector control register is used to initialize the 16-stage PRN generator to a specified starting point. The contents of the vector control register are loaded into the code generator register on the appropri command. Thus, the starting point of the pseudorandom sequence can b specified.

The final register, the serial output register, provides a means of reading out the current state of the code generator register. On the appropriate command, the contents of the PRN generator are loaded in parallel into the serial output register and clocked out in serial fashion. Each of these three registers has its own independent clock, permitting it to be devoted to other applications when not performing the above described functions.

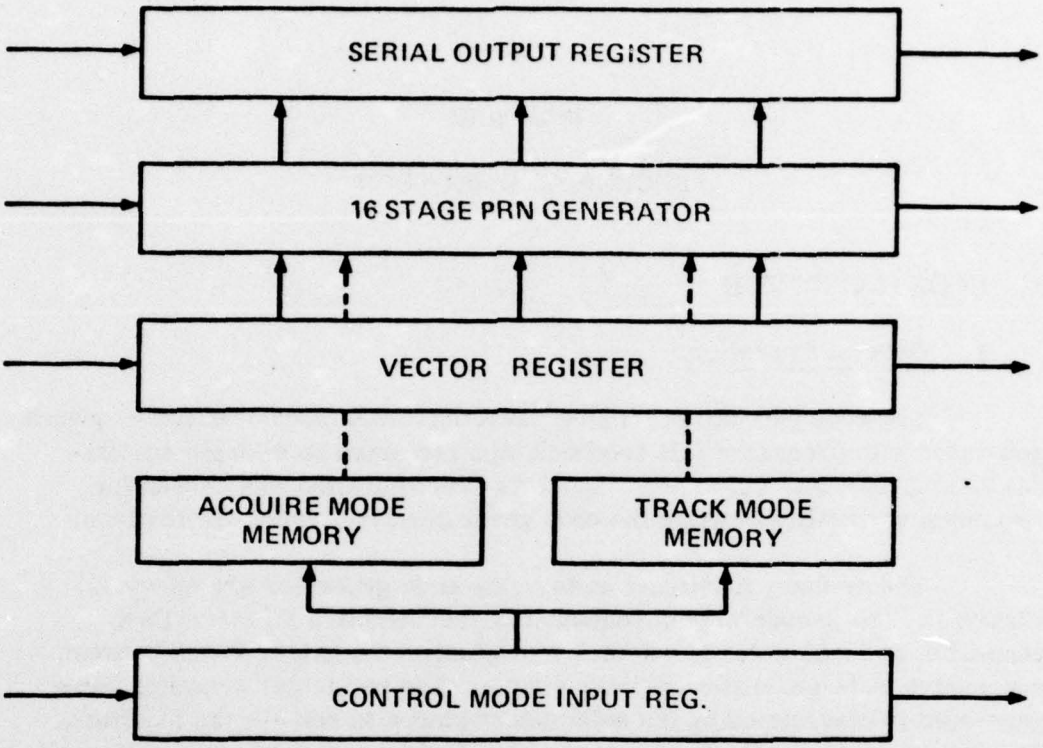


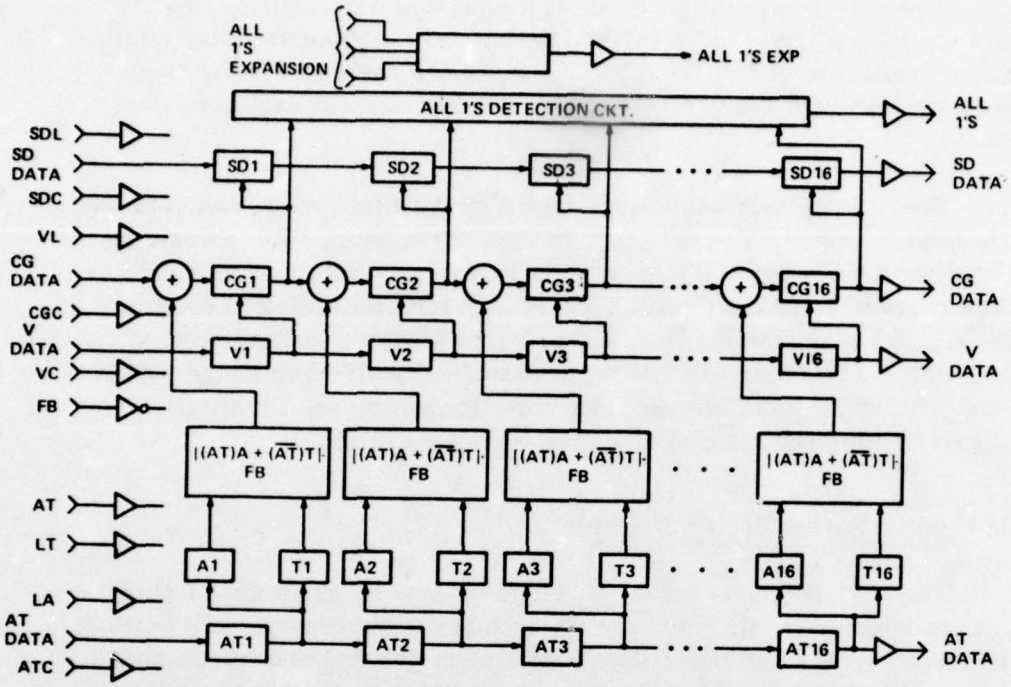
Figure 1. Primary functional units of the code generator.

The code generator array is designed to be fully expandable with longer code sequences being formed by connecting several arrays together. Each array thereby forms a 16-bit slice through the expanded code generator.

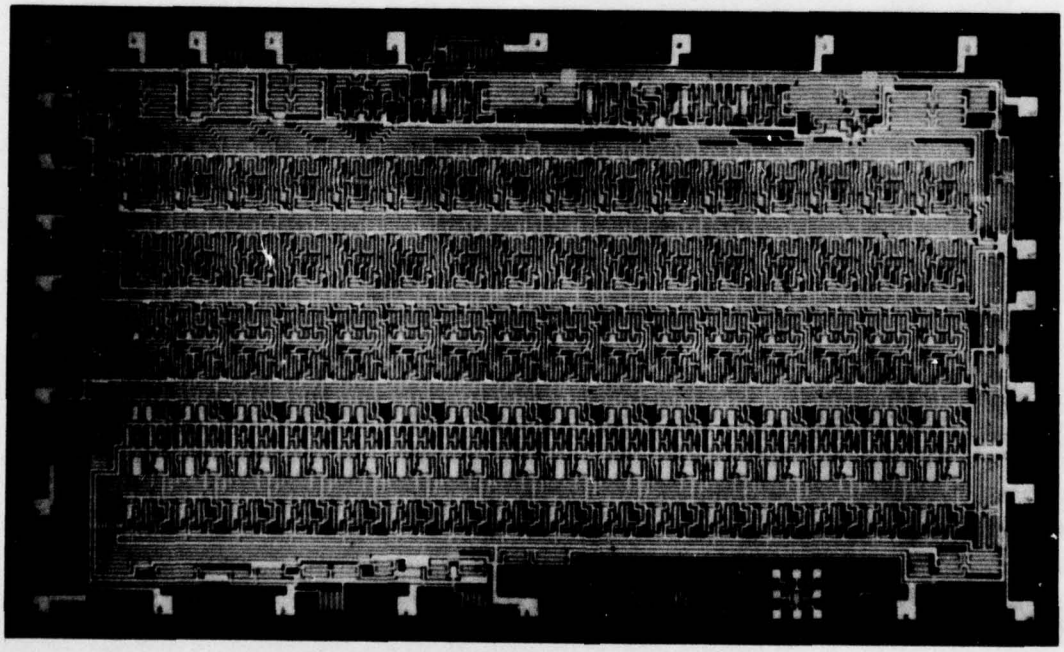
2. Array Description

a. Code Generator Register

The primary operational element of the TCS045 code generator array is the code generator (CG) register in which the pseudorandom code is formed. The CG register consists of 16 register stages, each with an exclusive OR on its input as shown in Figure 2. One input to each exclusive OR is the output of the previous register stage. The CG Data input to the array provides this input to the exclusive OR of stage one. The second input to each exclusive OR comes from the feedback selection circuitry which selectively gates the feedback, FB, input to those stages specified by the stored feedback tap pattern. The exclusive OR output is the input to the master/slave register of each stage. The state of the register in stage 16, the generated pseudorandom code, is made available on the CG Data output after passing through an output driver.



a. Functional block diagram.



b. Code generator photomicrograph.

Figure 2. 16-stage code generator (TCS045).

The code generator clock (CGC) input to the array provides the clocking for the CG register. Transitions in the register outputs occur on the positive going-transition of the clock pulse. Since the registers being used are quasi-static, the CGC clock is kept high whenever the CG register is not being clocked.

The CG register can be initialized by parallel loading the contents of the initialization vector, V, register into the CG register. This is accomplished whenever the VL input to the array is in the high state. The CGC input must be high or go high during the time VL is high for the loading to be completed. If CGC is low during the entire time VL is high, no loading occurs. Once loaded, the CG register will not respond to CGC until after VL goes low again. This parallel load feature provides a convenient means to initialize the CG register to any desired state at any time during operation.

b. Initialization Vector Register

The initialization vector, V, register is a 16-stage serial shift register. Data is entered into stage one through the V Data input. The state of stage 16 is made available on the V Data output after passing through an output driver. The clock signal for the V register is provided by the VC clock input. Output changes in the register stages occur when VC makes a transition from the low to the high state. The register stages used are quasi-static, being static only when VC is high.

The initialization vector register is used to initialize the CG register. The output of each stage of the V register is loaded into the corresponding stage of the CG register whenever VL is high. When it is not being used for initialization purposes, the V register is a 16-stage serial register that can be made available for other applications.

c. Serial Data Register

A 16-stage auxiliary output register called the serial data, SD, register is provided to enable readout of the current state of the CG register. Data is transferred in parallel fashion into the SD register from the CG register whenever the SDL input is high. For expansion purposes and to increase the versatility of the array, data can also be entered into the SD register in serial fashion through the SD Data input. The state of stage 16 is made available on the SD Data output after passing through an output driver. Thus, the SD register is a 16-stage serial register which can be loaded in parallel fashion from the CG register.

As is the case with the other shift registers in the TCS045 code generator array, the SD register has its own clock, SDC. All transitions in register states occur on the positive-going transition of SDC. Since the registers are quasi-static, SDC must be high when the SD register is not being clocked to prevent loss of information. Also, parallel loading is possible only while SDC is high. Once loaded in parallel fashion, SDL must be returned to the low state before the SD register is clocked.

The SD register provides for the high-speed readout of the states of the CG register, which is normally being clocked at a lower rate. This register can also be used as a 16-stage serial shift register independent of the rest of the array.

d. Acquire/Track Input Register

The acquire/track input (AT) register is a 16-stage serial shift register included on the code generator array for use in entering feedback tap position information into the storage registers. Data is entered into the AT register through the AT Data input, while the state of the 16th stage is made available on the AT Data output. The AT register has its own clock (ATC), making its operation independent of the rest of the array. All state transitions in the register occur on the positive-going transition of ATC. The quasi-static register stages used remain static only while ATC is high.

The feedback tap position information is entered in serial fashion on the AT Data input. The first bit entered is ultimately for the 16th stage of the CG register while the last bit entered is for the input stage. Once entered into the AT register, the tap position information may be transferred to either the A register if LA goes high or to the T register if LT goes high. As long as LA and LT are low, the AT register has no effect on the A or T register. This makes the AT register available for any other application requiring a 16-stage serial shift register once the feedback tap information is entered.

e. Feedback Selection Circuitry

The feedback selection circuitry is the portion of the array which takes the signal on the feedback input (FB) and selectively gates it to certain chosen exclusive ORs in the code generator register. This circuitry can be broken down into two parts, the storage registers containing the feedback tap position information and the feedback gating logic.

There are two 16-bit storage registers on the array, the A register and the T register. A "1" stored in a storage register cell denotes the presence of a feedback tap to the associated CG register stage. The absence of a feedback tap is denoted by a "0" stored in the storage register cell. The presence of two separate storage registers permits two different feedback tap patterns

to be stored at the same time. Thus, the code generator array can be used in applications requiring a short code for acquisition and a long code for tracking without having to enter new data into the storage registers when switching modes. The contents of one of the storage registers can be changed while the other is being used.

The entry of data into the A and T storage registers is from the AT input register using the LA and LT commands. The storage register used to define the feedback tap positions is specified by the AT input to the array. When AT is high, the A register is chosen, while the T register is chosen when AT is low. The input to the exclusive OR gate of each stage of the CG register is formed by ANDing the feedback input FB with the contents of the memory cell of the register selected by the AT input.

The A and T registers have a voltage input line (AT V_{DD}) which is separate from the rest of the array. This provides the user with the option of using the A and T registers as a nonvolatile storage. The only current which must be supplied by AT V_{DD} is the leakage current for the two registers plus a small dynamic current while changing code selection or storing a new code.

f. All 1's Detection Circuit

The presence of the all 1's state or unity vector in the code generator register is detected by the all 1's detection circuit. This circuit performs the AND operation on the outputs of the 16 stages in the CG register producing a 1 if and only if all register stages are in the 1 state. The all 1's signal is made available on the all 1's output after passing through two register stages. These register stages, which are clocked by the same clock as the CG register, delay the output of the all 1's signal by two clock periods. The all 1's signal serves as a convenient synchronizing point in observing a pseudo-random sequence produced by the code generator.

g. All 1's Expansion Circuit

The all 1's detection circuit detects the presence of the unity vector for a single chip. An all 1's expansion circuit is included on the array for use in detecting the all 1's state when several arrays are used together to form a longer code generator. Three inputs are provided to the all 1's expansion circuit. These three inputs are ANDed together to produce the all 1's expansion signal. This signal is retimed by a register clocked by CGC before it is made available on the All 1's Exp output. Thus, the expansion circuit on each array is capable of handling all 1's signals from three arrays. If more than three arrays are used in the expanded code generator, several of the expansion circuits must be used. It should be remembered that each time the signal passes through the all 1's expansion circuit, a delay of one clock period is introduced. If only two of the inputs are being used, the third input must be connected to V_{DD}.

h. Power Supply Requirements

The power inputs to the code generator array include two ground inputs and two separate positive voltage inputs. Both array ground inputs must always be connected to ground. The V_{DD} input supplies power to all the array except for the two memory registers with their associated LA, LT and AT control lines. These are supplied power by the AT V_{DD}. The use of a separate power input for the memory registers permits retention of the memory contents when the main power supply is off. The AT V_{DD} essentially only supplies the leakage current of the memory elements. The array is designed to operate over the full voltage range from 5 V to 15 V. Most arrays will operate down to lower than 3 V. The array will operate with up to several volts difference in the two power supplies. If the two separate power supply feature is not needed, V_{DD} and AT V_{DD} should be connected together.

i. Package Pin Designations

The code generator is packaged in a 28-lead DIP package of which 27 leads are used. The package pins along with their designation are as follows:

1.	Ground	15.	SDL
2.	(Unused)	16.	SDC
3.	ATC	17.	SD Data In
4.	AT Data Out	18.	Ground
5.	V_{DD}	19.	VL
6.	V Data Out	20.	FB
7.	CG Data Out	21.	CG Data In
8.	SD Data Out	22.	V Data In
9.	CGC	23.	VC
10.	Unity Vector Out	24.	AT
11.	Unity Vector Expansion Out	25.	AT Data In
12.	Unity Vector Expansion In	26.	AT V_{DD}
13.	Unity Vector Expansion In	27.	LA
14.	Unity Vector Expansion In	28.	LT

3. Array Operation

a. Clock Requirements

Four separate clock inputs are required by the code generator array. Each of these clock inputs provides clocking for only one of the four clocked registers in the array. The input clock signals are defined as follows:

1) CGC - code generator register clock
2) VC - initialization vector register clock
3) ATC - acquire/track input register clock
4) SDC - serial data output register clock.

The independent clocking of the four registers makes it possible to clock the different registers at different frequencies if required by various systems. The clocking of any one register has no effect on the other three registers.

All four clocked registers are of the quasi-static type. They maintain their state as long as the input clock remains high. Thus, whenever a register is not to be clocked, its clock input must be kept high. The quasi-static nature of the register stages also puts a minimum frequency limit on operation if a square-wave clock is used. Experimental results for the TCS045 indicate that this lower limit is less than 10 kHz. However, the registers may be operated all the way down to dc by using a clock signal which is low for less than 50 percent of the clock cycle.

All output transitions occur on the positive transition of the clock signal. Data clocked into the array is the data present on the input when the clock makes its positive-going transition.

The capacitive load seen by the source driving the clock input is minimized by using internal clock drivers. This load is approximately 3 pF on each of the clock inputs. The clock drivers in the array also reshape the clock signals and reduce any slow rise and fall times.

b. Initialization Techniques

Whenever the TCS045 code generator array is to be used to generate a pseudorandom code, the feedback tap information must be initially entered into the A and T registers. Feedback to a particular stage in the code generator register is enabled by a "1" stored in the corresponding cell of the selected A or T register. The A and T registers are loaded from the AT input register by the LA and LT inputs to the array. For example, each cell in the A register goes to the same state as the corresponding stage of the AT register whenever

LA is high. The feedback tap information must be initially entered into the AT register before being loaded into either the A or T registers. The entry of data into the AT register is serial with the first bit entered being the feedback tap information for the output stage of the code generator register. The loadings of the A and T registers are independent of each other except that both depend on the AT register for a source of data.

Using the initialization vector, V, register, the code generator register can be initialized to a predetermined starting point. The initial state is entered into the V register in serial fashion, beginning with the desired state of the output stage of the CG register. Loading from the V to CG register is parallel and is accomplished when the VL strobe is high.

The serial data SD register is initialized to the state of the CG register whenever SDL is high. This provides a means of reading out the current state of the CG register without disturbing its contents.

c. Code Generation

If the array is being used to generate a pseudorandom code, the CG Data output is connected to the FB input to provide the feedback signal. Once the initialization described above is accomplished, the only input required is the code generator clock, CGC. The code produced is available at the CG Data output. The CG Data input is normally maintained low while producing a PN code; however, different codes may be generated by maintaining the CG data input high or by applying a modulating signal to this input.

By appropriate programming of the feedback tap information, the effective length of the code generator register is selected to be any value from 1 to 16 stages. The effective length is determined by the feedback tap nearest the input end of the register. Register stages prior to the first stage with feedback do not enter into the PN code generation. For example, if a 10-stage code generator is desired, stages 1 through 6 of the A or T register selected will contain only "0's". A "1" would be stored in stage 7, with succeeding stages containing either "1's" or "0's".

d. Variable Length Shift Register

The code generator array can also be used as a serial shift register of any length up to a maximum of 64 stages. The acquire/track AT, initialization vector V and serial data output SD registers are each 16 stages long. By connecting the output of one of these registers to the input of another, the effective length is doubled to 32 stages. If all three of the registers are connected together, a register of length 48 is created, with outputs available after each 16 stages.

The code generator, CG, register can be programmed to look like a serial register with any length from 1 to 16 stages. A single "1" is programmed into the selected A or T register. If this "1" is at stage 1, the effective length is 16 stages. The effective register length decreases by one for each higher stage of the A or T register in which the "1" is stored. If the "1" is stored in stage 16 of the A or T register, the effective length is reduced to one stage. In this case, the register input is entered on the FB input rather than the CG data input. The ANDing of the FB input with the contents of the selected A or T register results in the FB signal being entered only into the CG register stage corresponding to the "1" in the storage register. If the CG Data input is kept low, the register functions as a normal shift register. However, if the CG Data input is high, the CG Data output is the FB input delayed by the specified number of clock periods and inverted. Thus, using the CG register in conjunction with the other three serial registers on the array, a serial shift register with either inverted or noninverted output and with any length from 1 to 64 stages is possible.

The operational speed of the individual registers is given in the section on array performance results. There is a slight maximum speed reduction from results obtained for the individual registers when they are connected together to form registers longer than 16 stages. This speed reduction is due to the delay through the array output drivers.

e. Storage Register Readout

Readout of data stored in the A or T storage registers requires the use of the CG register. The AT input is used to select the register to be read out. If AT is high, the A register is selected; while if AT is low, the T register is selected. The first step in reading out the selected storage register is to initialize the CG register to the all "0" state. This is done by either clocking the CG register with the CG data and FB inputs low, or by parallel loading the CG register with the all "0" vector from the V register. Once the CG register is in the all "0" state, the data is transferred from the storage register to the CG register by clocking the CG register once with the FB input high. With the FB input returned to the low state, the data can be clocked out on the CG Data output. An alternate approach is to parallel load the data into the SD register once it is in the CG register and then output it on the SD Data output.

f. Expansion Capabilities for Longer Codes

In many applications a pseudorandom code generator of more than 16 stages is required to generate the desired sequence length. The code generator array is designed for ease of expansion to meet such requirements. Two code generator arrays connected together form a code generator with a maximum of 32 stages. Each additional array added increases the maximum

number of stages available by 16, with each array forming a 16-stage slice through the expanded code generator. Expansion is achieved without sacrificing any of the capabilities of the code generator. Also, no additional logic is required when connecting the code generator arrays together.

Figure 3 shows three code generator arrays connected together to form a 48-stage code generator. The output of each of the four shift registers of the first array is connected to the corresponding register input of the second array. Similarly, the register outputs of the second array are connected to the register inputs of the third array. As a result, the effective length of each register is increased to 48 stages. In this case, the pseudo-random code is available at the CG Data output of the third array and is then connected to the FB input of each array to provide the feedback signal. The capacitive loading on the CG Data output resulting from driving a number of arrays is minimized by having the FB input drive only a single inverter on each array. Initialization procedures are the same for the expanded version as for a single array except that all register lengths are increased.

Each array contains a unity vector expansion circuit. The unity vector expansion circuit is used to AND the separate unity vector signals produced by each array to form the unity vector signal for the entire code generator. In the example of a 48-stage code generator, only one of these expansion circuits is used to AND the three separate unity vector signals. On longer code generators, several of the expansion circuits must be used. Each expansion circuit in the unity vector signal path introduces one clock period of delay.

The clock and load command inputs for the different arrays of the expanded code generator are the same.

4. Circuit Description and Design

a. Shift Register Stage Without Parallel Loading

Quasi-static register stages without parallel load capability are used in the initialization vector, V, and acquire-track, AT, registers. These register stages will retain data when clock is high, but loss of data can occur if clock is low for extended periods of time.

The operation of this register stage is explained by referring to the logic diagram of Figure 4. The input data, IN, is sampled when clock C is low, turning on transmission gate T1 and turning off transmission gates T2 and T3. This action applies the IN signal to the gate of inverter I1. The output of I1 is then $\overline{IN}$ and the feedback inverter I2 output goes to IN. The off transmission gate T2 isolates inverter I3 from changes in the I1 output. The

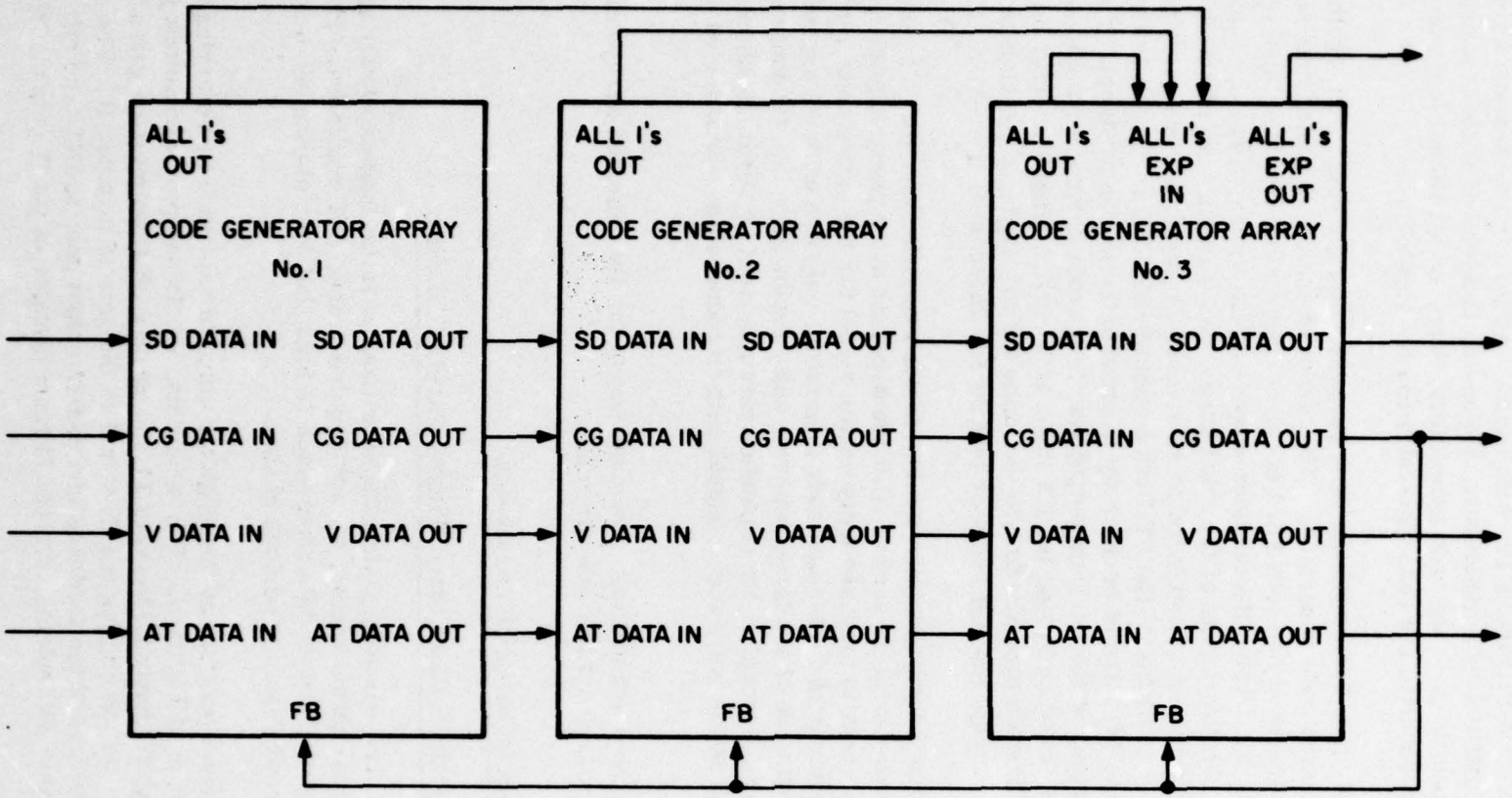


Figure 3. Three code generator arrays connected together to form a 48-stage code generator.

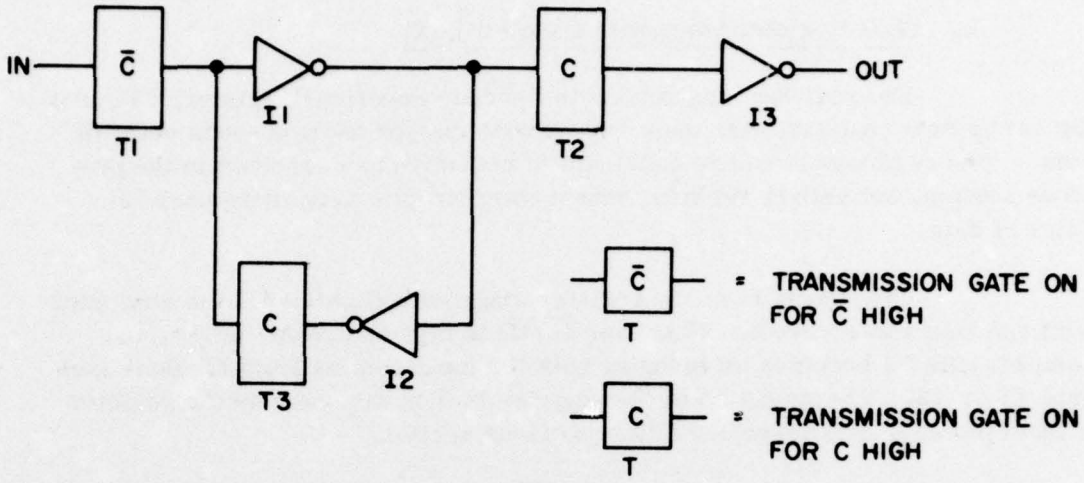


Figure 4. Shift register stage without parallel load.

gate voltage on I3 will remain constant unless leakage current charges or discharges the gate capacitance. The rate at which this gate capacitance is charged or discharged by leakage determines the maximum time clock can remain low without the register malfunctioning.

When clock goes high, transmission gate T1 is turned off and transmission gate T3 is turned on which places the output of I2 on the input to I1. T1 isolates the register from any further changes which may occur in IN. The feedback devices I2 and T3 maintain the same voltage on the gates of I1 as established prior to clock transition preventing any change due to leakage. At the same time, transmission gate T2 is turned on which places the output of I1 on the input of I3. The resulting output signal, OUT, becomes the same as the IN signal sampled when clock was low. These voltages are maintained indefinitely as long as clock remains high.

The shift register stage could be made static when C is low by placing a feedback inverter and transmission gate around I3. However, this would increase the number of devices in the register stage from 12 to 16 with a corresponding increase in array area. Also, the additional logic would result in a slight decrease in the maximum clock rate for the register. Another possibility considered during the design phase was to eliminate T3 and use devices with high length to width ratio in I2. The resulting cell area saved is minimal and this design is more subject to problems if extreme variation in process parameters occurs.

b. Shift Register Stage with Parallel Load

The register stages used in the code generator register, CG, and the serial data register, SD, must have provisions for asynchronous entry of data. The registers used are quasi-static registers as described in the previous section, but with I1 replaced with a complex gate permitting parallel entry of data.

The operation of the register stage with parallel load is explained with reference to Figure 5. Whenever $\overline{\text{LOAD}}$ is high and LOAD is low, the complex gate G1 becomes an inverter with the input coming from transmission gate T1 or T3. The operation of the register is then the same as the register without parallel load described in the previous section.

When LOAD is high and $\overline{\text{LOAD}}$ is low, the gate G1 looks like an inverter with LOAD DATA as its input. If clock is high turning on T2, the register output, OUT, will become the same as the LOAD DATA input. The feedback loop will be closed when LOAD goes low, and the register will be held in the state established while LOAD was high. Proper operation requires that the clock C be high whenever a parallel load takes place. In an attempt to parallel load with clock C low, the off transmission gate T2 will keep the LOAD DATA input from reaching the output. When LOAD goes low the output of G1 will go to IN rather than LOAD DATA since T1 is on and T3 is off.

The register stage with parallel load requires 18 devices as compared with the 12 devices required without parallel load. The maximum clock rate for the register is only slightly reduced from that of register without parallel load.

c. Storage Register

The storage register used in the A and T registers is the third type of register used in the code generator array. The lack of a serial shift requirement simplifies the register structure and reduces the number of devices to 8.

The operation of the storage register is explained by referring to Figure 6. Whenever clock L is high, transmission gate T1 is turned on while T2 is turned off. The output signal OUT will go to the same state as the input signal IN. When L goes low, T1 is turned off isolating the register from any further changes in IN, while T2 is turned on completing the feedback loop. Neither inverter input is free to drift resulting in full static storage.

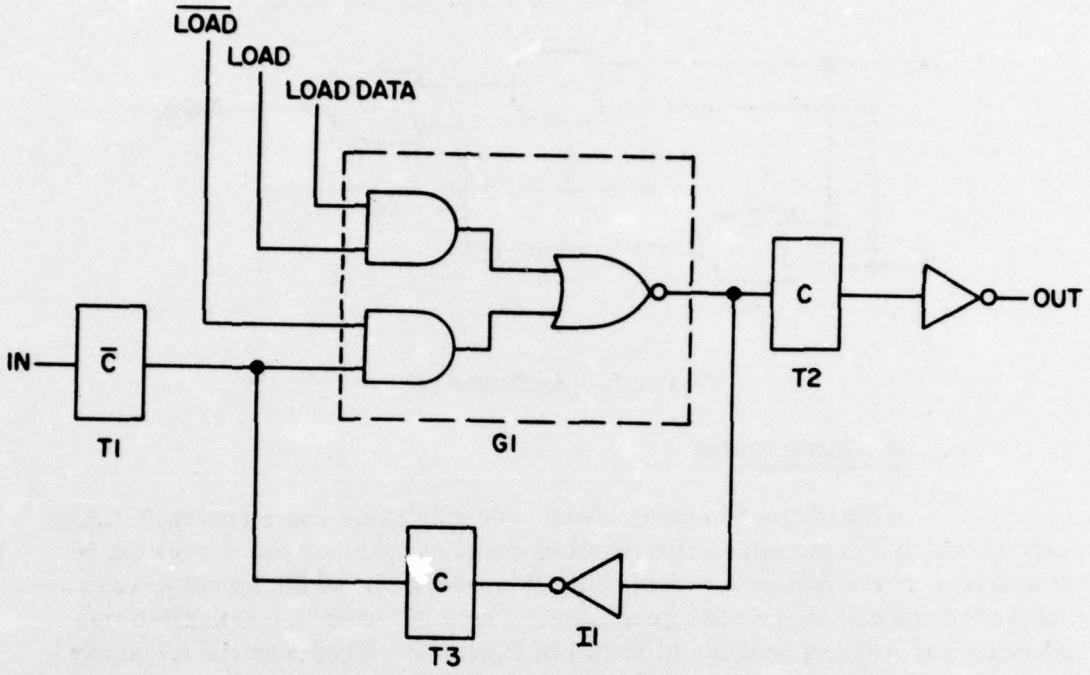


Figure 5. Shift register stage with parallel load.

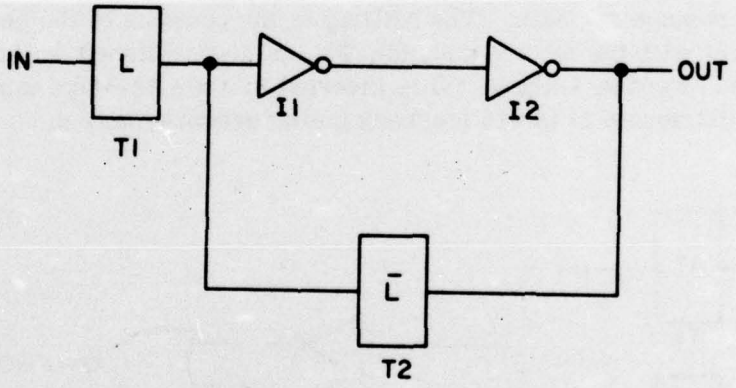


Figure 6. Storage register.

d. Exclusive OR

The code generator register portion of the array requires 16 exclusive-OR gates in addition to the register stages with parallel load. Of the several possible circuits for the exclusive-OR function, the one shown in Figure 7 was chosen. This exclusive OR produces only two gate delays, has a total of 10 devices, and requires only the uncomplemented form of the input signals.

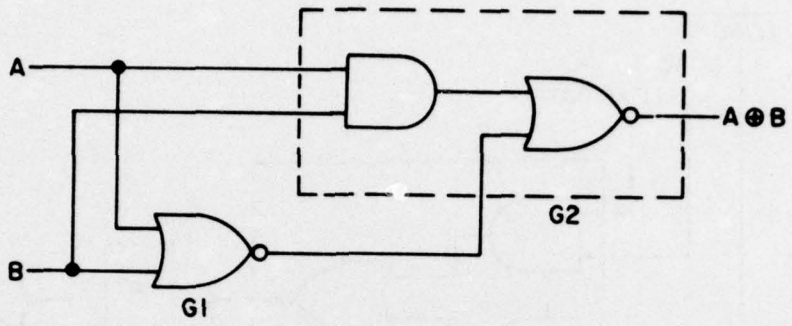


Figure 7. Exclusive OR.

e. Feedback Gating

Each of the 16 stages of the code generator has a feedback gating network which selects either the output of the A register or the T register to be ANDed with the feedback signal, FB, to produce one of the inputs to the exclusive OR located in the code generator. The logic used to accomplish this selection and ANDing process is shown in Figure 8. Whenever the AT array input is high, transmission gate T1 is turned on while transmission gate T2 is turned off thereby selecting the contents of the A register. Conversely, whenever AT is low, T2 is turned on while T1 is turned off thereby selecting the contents of the T storage register. The ANDing of the contents of the selected storage register with the feedback signal, FB, is accomplished by gates G1 and G2 of Figure 8. Feedback signal FB is inverted in a single-stage input driver before being distributed to the 16 feedback gating networks as $\overline{FB}$.

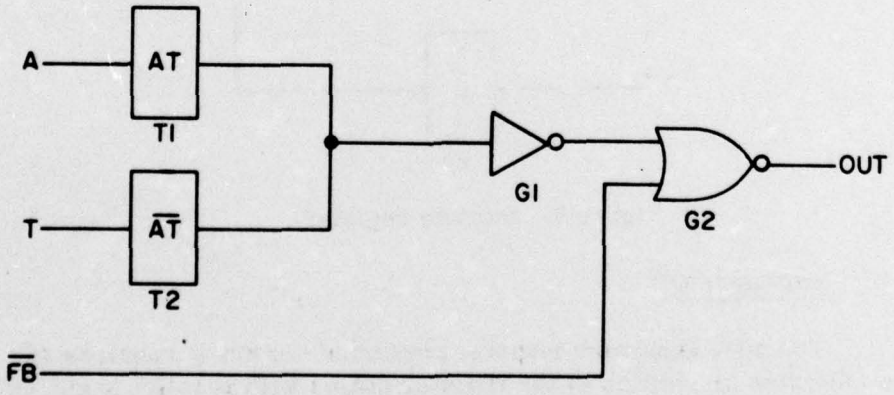


Figure 8. Feedback gating network.

Of prime concern in the design of the feedback gating network is the minimization of delay in the path from the FB input. This is the critical path in determining the maximum frequency of operation of the code generator. As designed, there are only two gate delays between the FB input to the array and the exclusive-OR gates, namely, 1) the FB input driver which minimizes the capacitive load seen at the input and 2) a two-input NOR in the feedback gating network.

f. All 1's Detection Circuit

The all 1's detection circuit detects the presence of the unity vector in the CG register by ANDing the states of the 16 register stages. The circuit used for this purpose is shown in Figure 9. The inputs are broken down into two groups of eight to simplify the array layout and to minimize the throughput delay. The use of two input NAND and NOR gates keeps device size requirements to a minimum while maintaining speed. The two signals formed by NANDing each group of eight inputs are retimed in a register stage before being combined in a NOR gate. The output of the NOR gate is retimed in another register before going to the All 1's output driver. The net effect of this logic is to AND the 16 input signals while introducing two clock periods of delay. The retiming registers used are identical to the registers without parallel load previously described. The clock signal for these registers is CGC, the clock for the code generator register. As a result of the retiming registers, transitions in the All 1's output coincide with transitions in the CG Data output.

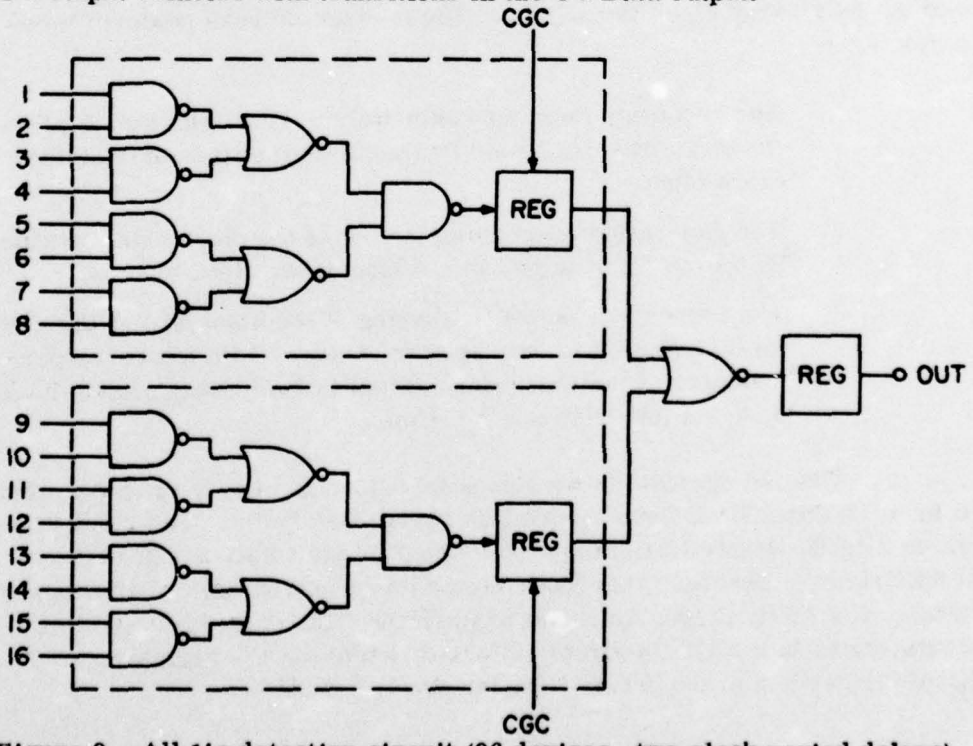


Figure 9. All 1's detection circuit (96 devices, two clock period delays).

g. All 1's Expansion Circuit

The all 1's expansion circuit is used to combine the outputs of the all 1's circuits from several chips to produce an overall unity vector signal when several chips are used to form an expanded code generator. The all 1's expansion circuit, shown in Figure 10, consists of a three input NAND gate, inverter and retiming register. The three inputs are ANDed and given a one clock period delay by the register. The retiming register is the register without parallel load previously described. The clock signal for this register is CGC, the code generator register clock.

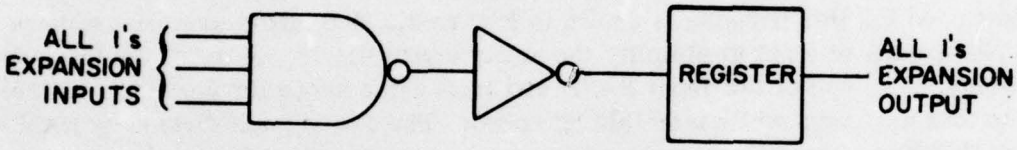


Figure 10. All 1's expansion circuit.

h. Input and Clock Drivers

Input clock drivers of the type shown in Figure 11 are used on each of the four array clock input lines. These clock drivers perform three main functions:

1. The reduction from approximately 9 pF to less than 3 pF in the capacitive load seen by the off chip source driving the clock input.
2. The generation of the complement of the clock signal required by the register stages in addition to the clock signal.
3. The reconstitution and reshaping of the clock signal prior to its distribution to the register stages. This improves performance if the input clock signal is less than full amplitude or has a long rise and fall time.

The use of clock drivers does introduce a delay in the clock signal which must be considered from the system timing standpoint. The clock signal on chip is slightly delayed from the $\overline{\text{clock}}$ signal by the additional inverter in the clock driver. However, this clock skew is not great enough to affect array operation. A slightly larger driver is used on the CGC clock input since it clocks registers in the all 1's circuitry in addition to the CG register. The widths of the devices in the driver inverter are listed below.

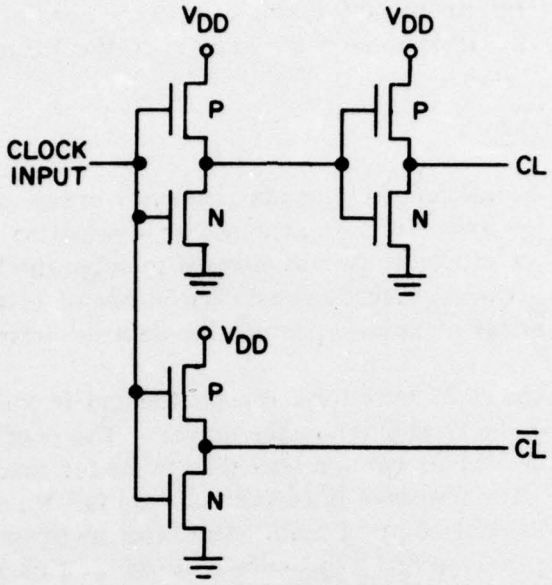


Figure 11. Clock driver.

Clock Driver	P Device Width	N Device Width
CGC	21 mils	14 mils
VC	17.1 mils	11.4 mils
SDC	17.1 mils	11.4 mils
ATC	17.1 mils	11.4 mils

Input drivers are also used on the LA, LT, AT, VL, and SDL control inputs. Each of these control signals and its complement is required by the 16 stages of the array. The use of a driver on these inputs also provides signal reshaping and a reduction in the input capacitive load. The drivers used for these inputs are the same as the clock drivers except that reduced loads permit device size reduction to a 13.5 mil width for the p-device and a 9 mil width for the n-device.

No input drivers are used on the data inputs to the four registers. In each of these cases, the array input goes to just the input stage of the register, and hence, the capacitive load is small. Also, a driver on these inputs would delay the input signal thereby reducing the maximum speed when more than one TCS045 array was used.

An input driver consisting of a single inverter is used on the FB input. Since the feedback signal path is the critical path in determining the maximum operating rate of the code generator, it was desired to keep the capacitive load seen by the input and any driver delay to a minimum. Also, $\overline{FB}$ rather than FB is required as the input in the feedback selection circuitry.

To best satisfy all these requirements, a single inverter consisting of a 10.8 mil wide p-device and 7.2 mil wide n-device is used on the FB input.

i. Output Drivers

Device sizes internal to the code generator array are kept small to minimize both the array area and the array power dissipation. However, these small devices do not supply sufficient current to drive the larger capacitive loads seen off-chip. Output drivers consisting of two inverters in series are used on each of the array outputs to provide the desired drive capability.

Device widths of 27 mils for the p-device and 18 mils for the n-device were chosen for the final stage of the driver. The predicted output rise and fall times for this driver remain less than 20 ns for loads up to 35 pF when operating at 10 V. The increase in output rise and fall times is approximately 4 ns for each additional 10 pF of load. The input inverter in the output driver has a 9 mil wide p-device and 6 mil wide n-device. This inverter is intermediate in size between the register output inverter and the final driver inverter. It is capable of driving the load presented by the final driver inverter without excessively loading down the register output.

5. Array Performance

The performance information presented in this section was obtained from tests performed on packaged code generator arrays at RCA Advanced Technology Laboratories.

a. Maximum Speed as Code Generator

The code generator array is designed to produce a 20-megabit-per-second pseudorandom sequence when operating at 10 V. The maximum speed is measured with the array producing a maximal length sequence of $2^{16} - 1$ bits length. The maximal length sequence used is obtained by programming feedback taps to stages 1, 3, 4, and 6. Speed results do not depend on whether the A or T mode is selected. The maximum speed is independent of the code being generated or the effective length of the code generator.

The maximum speed at various operating voltages is given in Table 1. The load on the CG Data output consists of the FB input, the test fixture, and the scope probe used to observe the output. The test fixture and scope probe contribute 3 to 5 pF to the load. The maximum speed obtainable showed variation from one processing run to another. All the arrays which did not exceed 20 MHz at 10 V are from the same lot. The distribution of maximum speeds at 10 V for the arrays tested is given in Figure 12. The plot of maximum frequency versus operating voltage (see Figure 13) shows that the

TABLE 1. MAXIMUM CODE GENERATOR SPEED GENERATING A PN SEQUENCE

V_{DD} (V)	Maximum Clock Rate (MHz)		
	Average	Minimum	Maximum
3	3.9	2.6	7.8
5	10.4	8.4	16.6
7	15.5	12.6	22.7
10	22.1	17.8	30.7

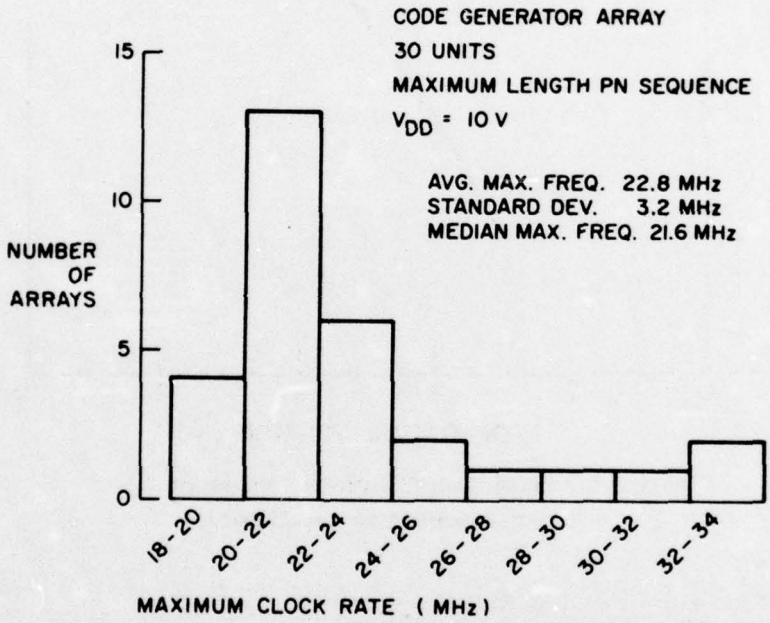


Figure 12. Distribution of maximum speeds at 10 V for the arrays tested.

maximum operating rate of the code generator increases nearly linearly with the supply voltage.

The speed at which a pseudorandom sequence can be generated also depends on the capacitive load on the CG register output. Increasing the capacitive load on the output increases the output rise and fall times. Since the CG register output is connected to the FB input, increased delay is introduced in the feedback path whenever the output rise and fall times increase. The effect of the capacitive load on the maximum speed is minimized by using a driver stage on the register output. Figure 14 is a plot of the maximum code generator frequency as a function of load when operating at 10 V.

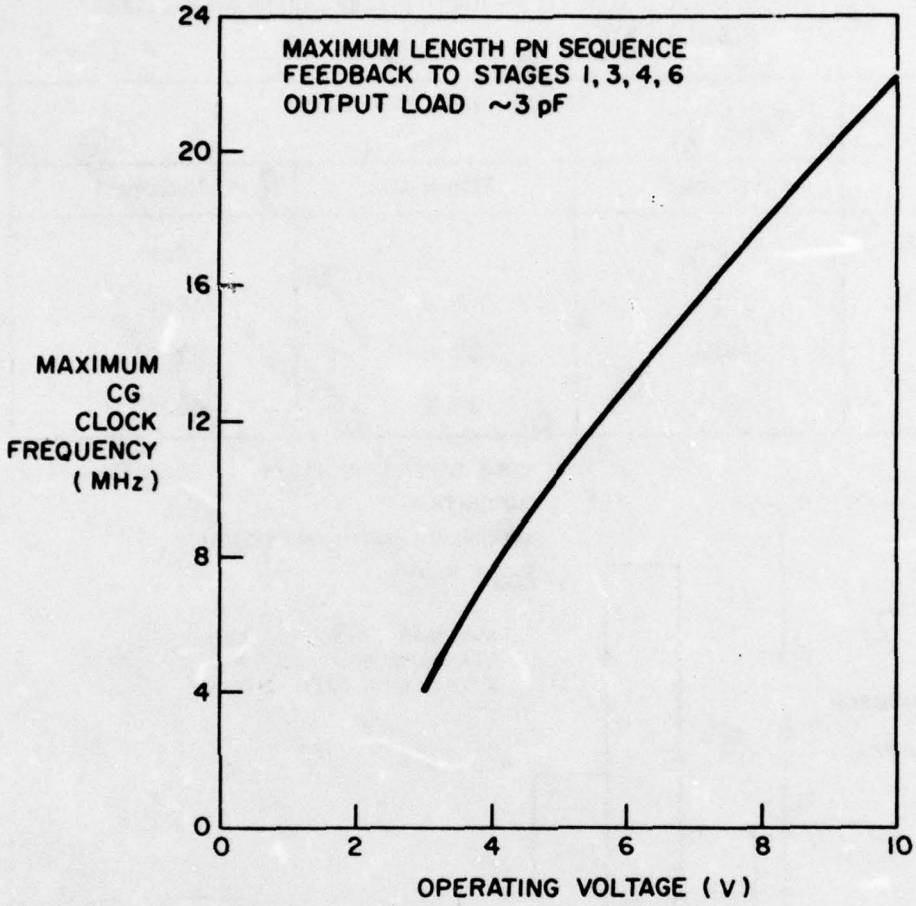


Figure 13. Maximum CG clock frequency versus operating voltage.

b. Maximum Speed as Shift Register

The maximum speed of the CG register when operated as a 16-stage shift register is twice that obtainable when it is operated as a pseudorandom sequence generator. The maximum speed as a pseudorandom sequence generator is limited by delay through the output driver, the FB input driver, and the feedback gating network. The limiting factor when operated as a shift register is the maximum rate at which the register stages themselves can be clocked. The average maximum clock rate for the registers is given in Table 2.

The CG and SD registers have identical stages with the parallel load feature. The difference in speed between these two registers is primarily due to the presence of an exclusive-OR gate between successive stages of the CG register. Register stages without the parallel load feature are used in the AT and V registers. This simplification in the logic increases the speed of these registers over that of the SD register. The slight difference in speed

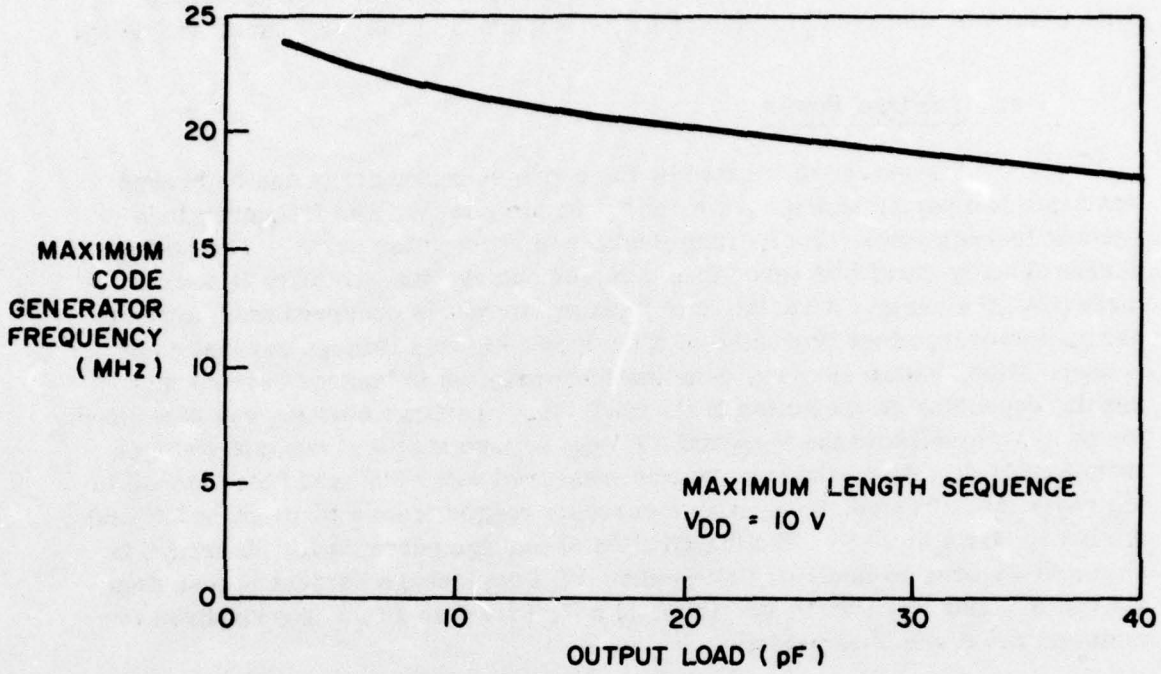


Figure 14. Maximum code generator frequency as a function of load when operating at 10 V.

TABLE 2. MAXIMUM CLOCK FREQUENCY FOR SHIFT REGISTERS

Register	Maximum Clock Rate (MHz)		
	V_{DD} = 5	V_{DD} = 7	V_{DD} = 10
CG	20.5	31.9	44
SD	34.7	*	*
AT	40.2	*	*
V	38.7	*	*
*Greater than 50 MHz			

between the AT and V registers can be attributed to a difference in the load each must drive in the array since they are identical in other respects.

The maximum speeds given above are determined solely by the internal operation of the registers. In any application of the registers, the delay introduced by the output drivers would have to be taken into consideration. The delay in the output drivers will reduce the maximum speed when several

of the registers are connected together. However, the output drivers are needed to reduce the effect of output load capacitance on register performance. This is further discussed in the section of output rise time, fall time, and delay.

c. Leakage Power

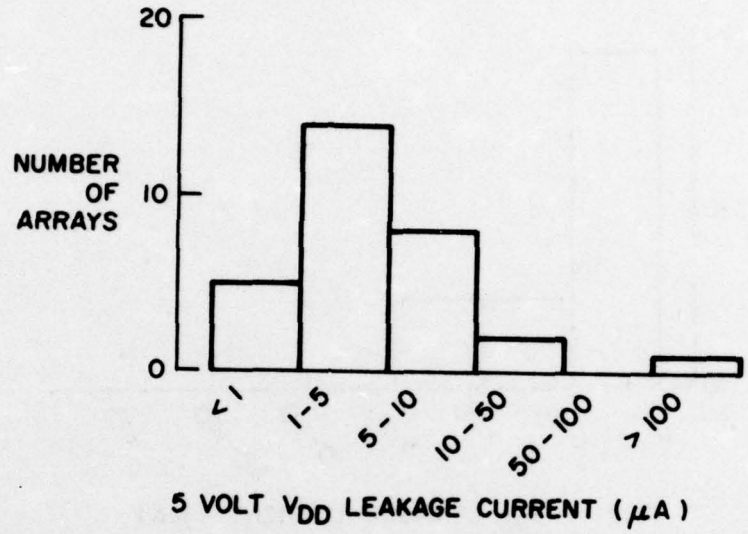
The power dissipated by the code generator array can be broken down into two parts, leakage power and dynamic power. The frequency independent leakage power results from leakage current in the array. The leakage current ideally should be zero since complementary MOS circuitry is used throughout the array. A variation in leakage current is observed from array to array, however, since normally OFF devices do have a leakage current component. Also, within an array considerable variation in leakage current may result, depending on the states of the registers. Leakage current was measured for each array on both the V_{DD} and AT V_{DD} voltage inputs at several voltages from 3 to 10 V. Also, the leakage was measured with "0's" and "1's" stored in the registers. Typical V_{DD} leakage currents ranged from 1 to 10 μA at 5 V and from 1 to 50 μA at 10 V. The distribution of leakage currents for 30 arrays is shown in Figures 15 and 16. The median AT V_{DD} leakage current is less than 2 μA at 5 V and 10 μA at 10 V. Thus, at 5 V, less than 10 μW are required to maintain the A and T registers.

The protection diodes on the signal inputs consisting of four stacked zener diodes will draw a small current when the input signal is in the high state. This leakage becomes significant only at the upper operating voltages. The input leakage was measured to be approximately 2.3 μA per input when the input is at 10 V.

d. Dynamic Power

The dynamic power is a direct function of the speed at which the array is operated. If none of the logic circuitry is changing state, the only power is the leakage power. The dynamic power measured in milliwatts per megahertz for the array when generating a maximum length pseudorandom sequence is given in Table 3. The sequence is produced by feedback to stages 1, 3, 4, and 6. Only the code generator clock CGC is being clocked, all other registers being maintained constant. The output load is the 3 to 5 pF of the test fixture and scope probe. For a shorter sequence which uses fewer stages of the CG register, the dynamic power will be lower. These results show that the code generator operating at 10 V will produce a 20 megabit per second sequence with a power dissipation of approximately 106 mW. These dynamic power results are also plotted in Figure 17.

Dynamic power dissipation for each of the four registers when operated as a shift register is given in Table 4, with results for the CG and SD also plotted in Figures 18 and 19. The dynamic power was measured with all "0's"



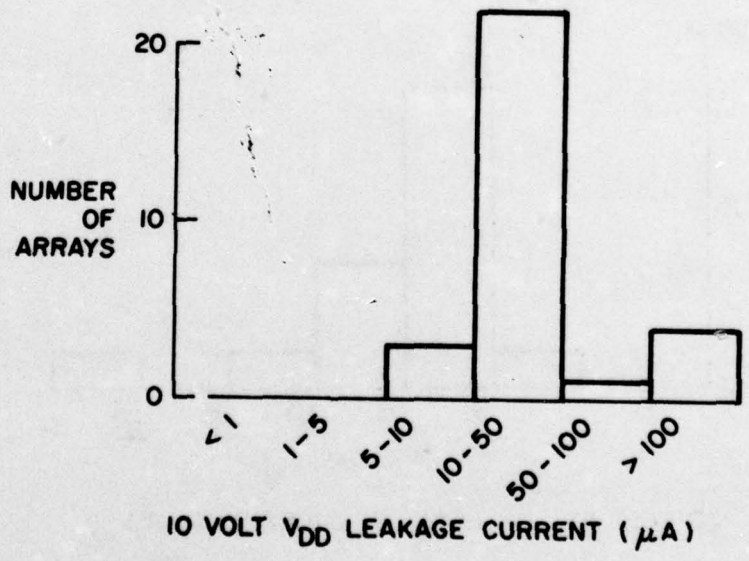
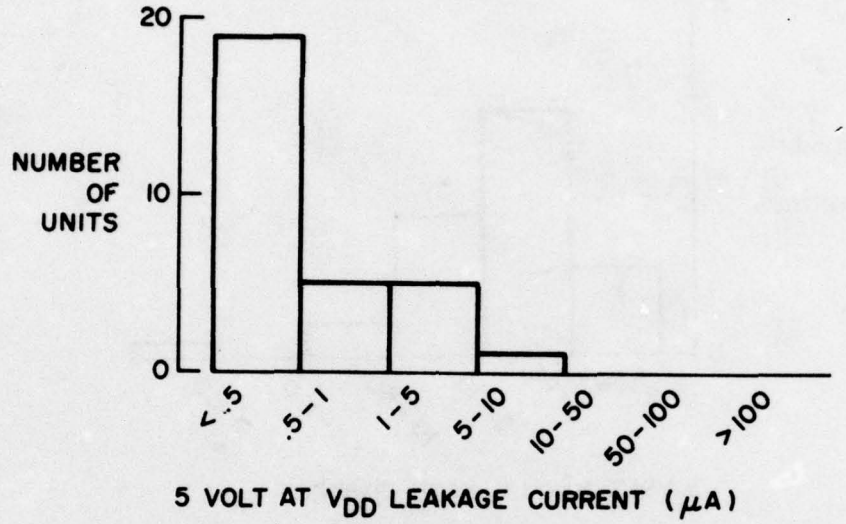


Figure 15. TCS045 total array leakage current histograms.



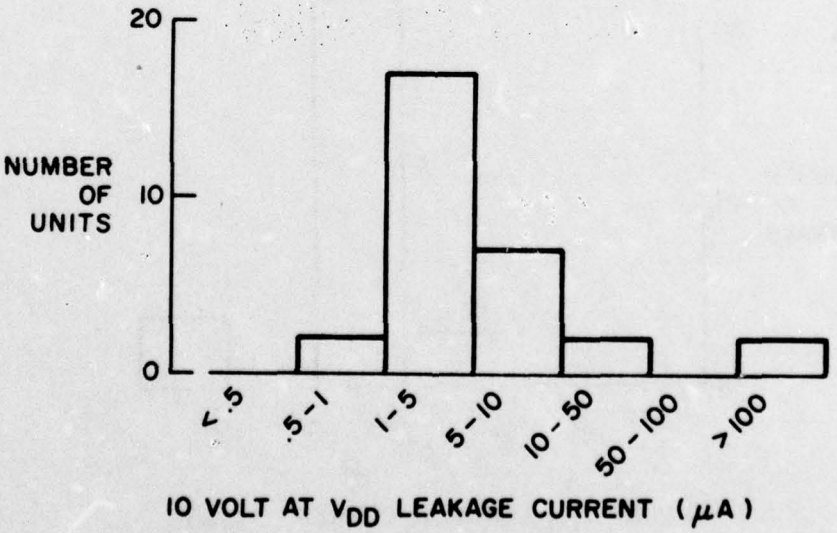


Figure 16. Acquire/track (AT) memory leakage current histograms.

TABLE 3. DYNAMIC POWER WHILE PRODUCING MAXIMAL LENGTH SEQUENCE

Voltage (V)	Dynamic Power (mW/MHz)
3	0.4
5	1.16
7	2.42
10	5.30

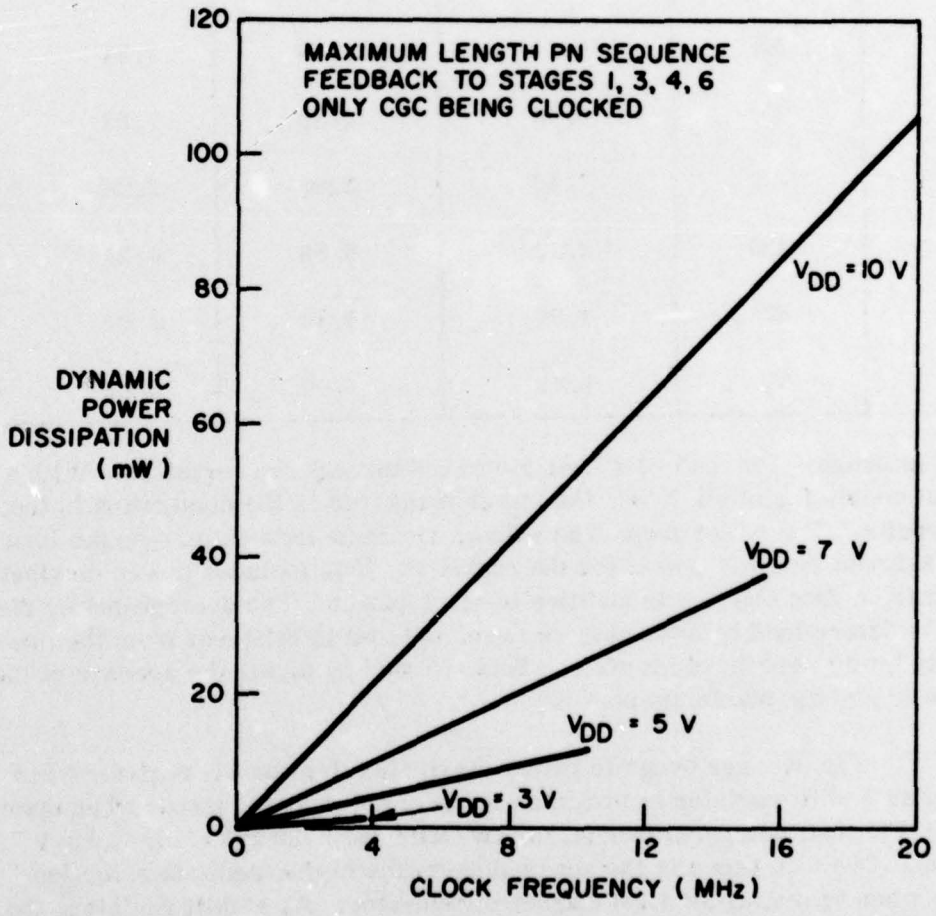


Figure 17. TCS045 dynamic power results.

TABLE 4. SHIFT REGISTER DYNAMIC POWER

V_{DD} (V)	Register	Dynamic Power (mW/MHz)		
		Clock Only	Maximum	Average
5	AT	0.34	0.84	0.59
	CG	0.50	1.43	0.96
	SD	0.36	0.87	0.62
	V	0.40	0.88	0.64
7	AT	0.69	1.74	1.21
	CG	1.00	3.01	2.01
	SD	0.74	1.88	1.31
	V	0.80	1.85	1.32
10	AT	1.45	3.83	2.64
	CG	2.12	6.55	4.34
	SD	1.56	4.18	2.87
	V	1.69	4.06	2.87

and with alternate "1's" and "0's" being clocked through the registers. With a data input consisting of all "0's", the power measured is the dissipation in the clock circuits. The power measured with an alternate data pattern on the input is the maximum dynamic power for the register. This includes power dissipation resulting from data changes in addition to clock power. The average power dissipation is determined by assuming that each data bit is different from the previous data bit 50 percent of the time. This is found by taking the average of the clock power and the maximum power.

The average dynamic power dissipation for the CG register when operating as a shift register is less than the average dynamic power when operating as a PN sequence generator (4.34 mW/MHz vs. 5.30 mW/MHz at 10-V operation). The difference is the power dissipation in the feedback selection circuitry when operating as a PN sequence generator. As a shift register, the power dissipation for the CG register is greater than the dissipation of the other three registers. The additional power results from the exclusive-OR gates

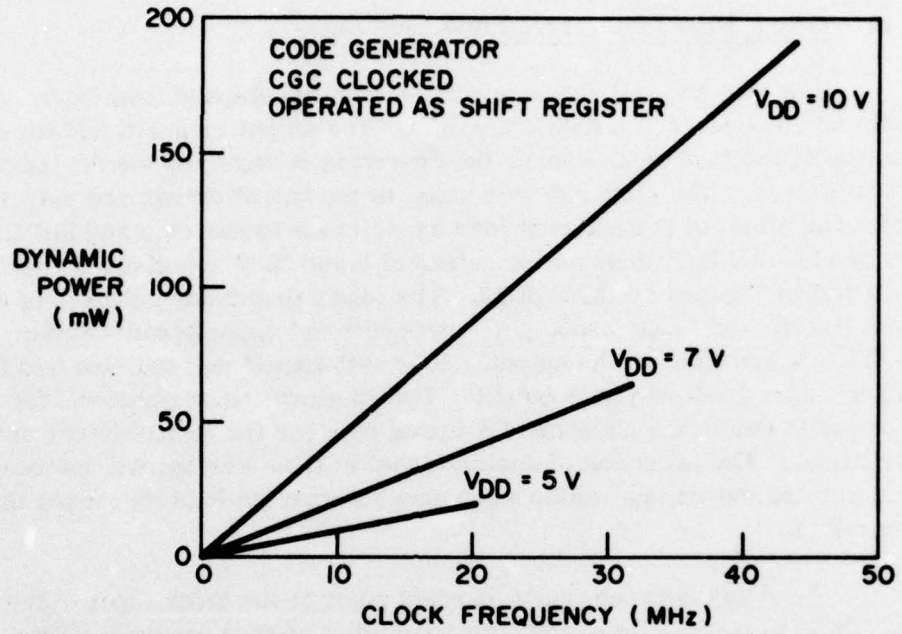


Figure 18. TCS045 speed-power curves (CG operated as shift register).

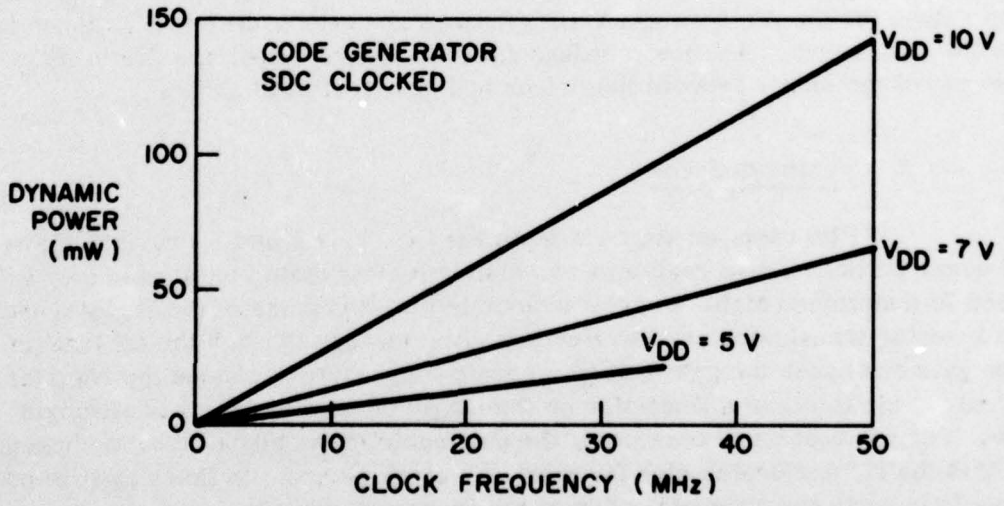


Figure 19. TCS045 speed-power curves (serial data register).

between CG register stages and from the CGC clock also being used to clock registers in the all 1's circuitry and all 1's expansion circuitry.

e. Output Rise Time, Fall Time, and Delay

The rise and fall times are defined as the elapsed time between the 10 percent and 90 percent of a data transition. The output rise and fall times are a function of the load capacitance, the operating voltage and the device sizes in the output driver. The larger device sizes in the output driver are selected to minimize the effect of the external load capacitance on the rise and fall times. The average rise and fall times as measured at 5 and 10 V are given in Table 5, and are plotted in Figures 20 through 23. The load capacitance consists of 5 pF for the test fixture and scope probe plus any additional capacitance. Since identical drivers are used on the outputs, it is anticipated that the rise and fall times will not vary from output to output. The smaller values observed for the SD Data output is due to the absence of a tunnel between the output driver and pad on the array. The presence of such a tunnel in the other outputs introduces resistance into the output lead which when coupled with the load increases the RC time constant.

The delay between the 50 percent point of the clock input to the array and the 50 percent point of the output transition was measured. This delay includes the delay of the clock driver, the output portion of a register stage, and the output driver. The logic circuitry involved in this delay path is shown in Figure 24. The input clock signal used has rise and fall times of 6 ns. Average delay values as a function of load capacitance at 5 and 10 V are plotted in Figures 25 and 26 and given in Table 6 for the CG Data and SD Data outputs. The values for the AT Data and V Data outputs are nearly the same as those for the CG Data output. The lower values for the SD Data output are due to the absence of the tunnel between the driver and pad mentioned above.

f. Minimum Speed

The register stages used in the CG, V, AT and SD registers are all quasi-static. These registers can maintain their state indefinitely only when clock is maintained high. whenever clock is low, the gates of the register output inverter transistors are left floating. Any leakage through the off transmission gate can cause the gate voltage to change and thereby change the register output. This imposes a limitation on the length of time the clock can remain low. For low frequency operation, the duty cycle of the clock must be chosen so that the clock remains high for most of a clock period. In this way it is possible to operate the code generator at any frequency down to dc.

The length of time the clock can remain low is determined by measuring the minimum frequency at which the registers will operate using a square wave clock. This minimum operating frequency showed considerable variation

TABLE 5. CODE GENERATOR OUTPUT RISE AND FALL TIMES

Output	Load (pf)	Rise Time (ns)		Fall Time (ns)	
		At 5 V	At 10 V	At 5 V	At 10 V
AT Data	5	17	8	11	7
	15	32	16	20	12
	23	39	20	26	14
	38	59	33	40	22
	61	84	48	58	32
CG Data	5	20	10	14	7
	15	36	19	24	13
	23	43	23	28	16
	38	61	35	41	23
	61	86	49	58	33
SD Data	5	12	6	9	5
	15	27	13	16	8
	23	35	17	20	10
	38	53	26	31	16
	61	78	40	45	24
V Data	5	13	7	11	6
	15	30	16	20	11
	23	37	19	25	14
	38	56	30	38	22
	61	85	45	55	33

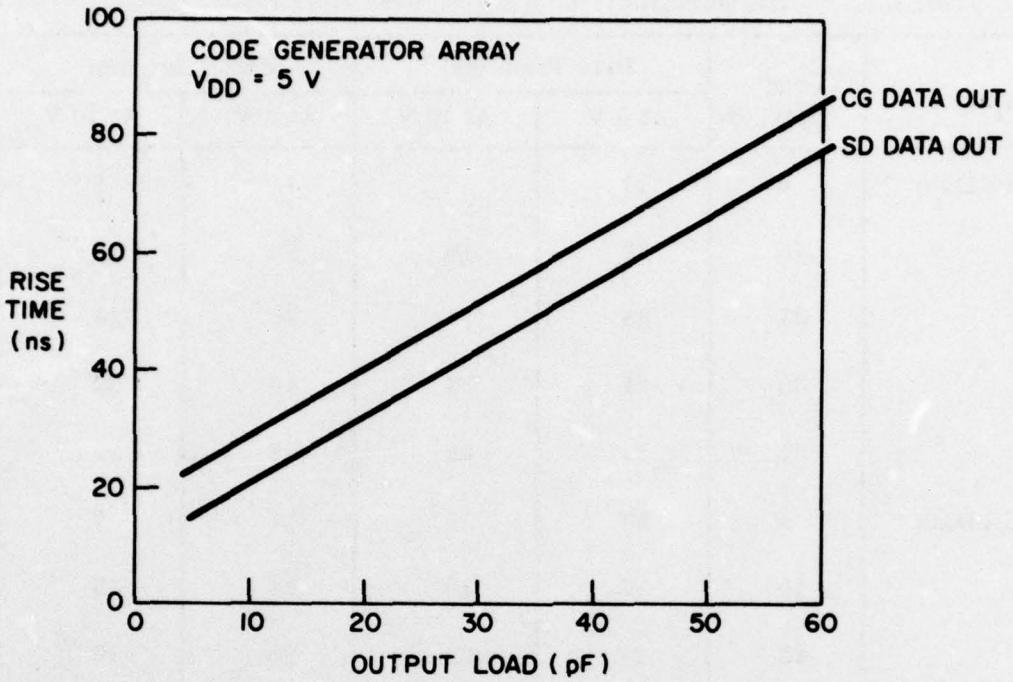


Figure 20. TCS045 average output signal rise time at 5 V.

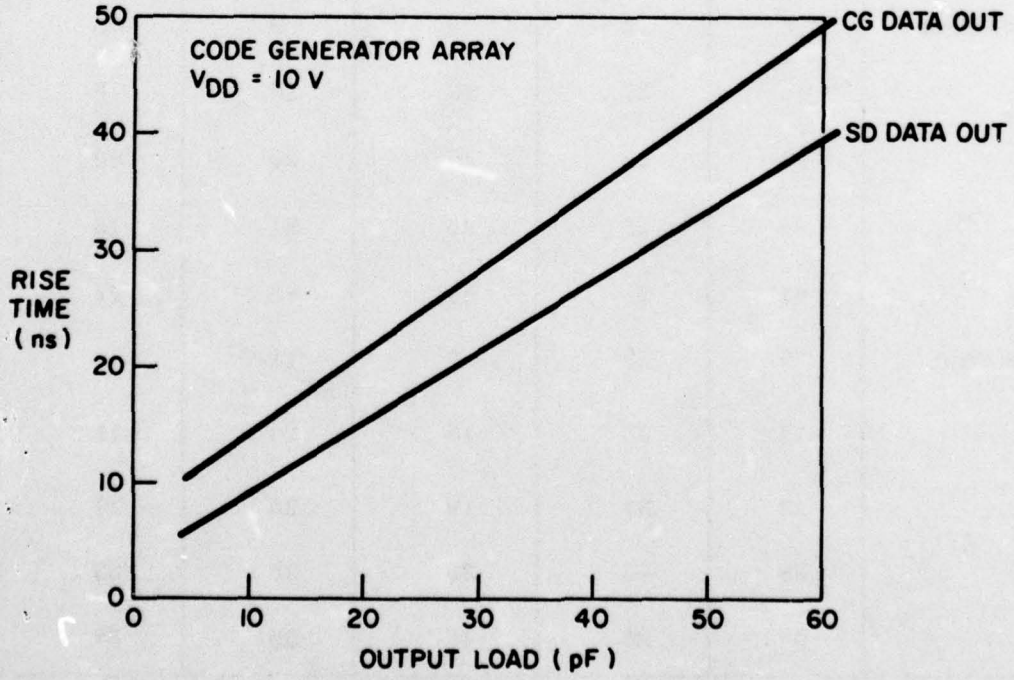


Figure 21. TCS045 average output signal rise time at 10 V.

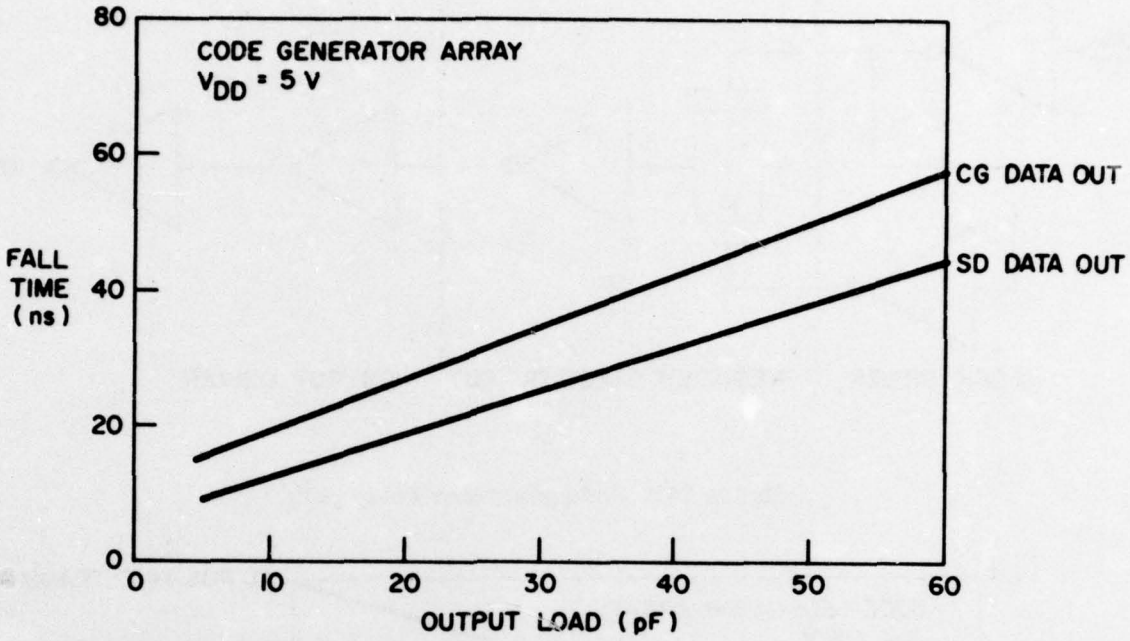


Figure 22. TCS045 average output signal fall time at 5 V.

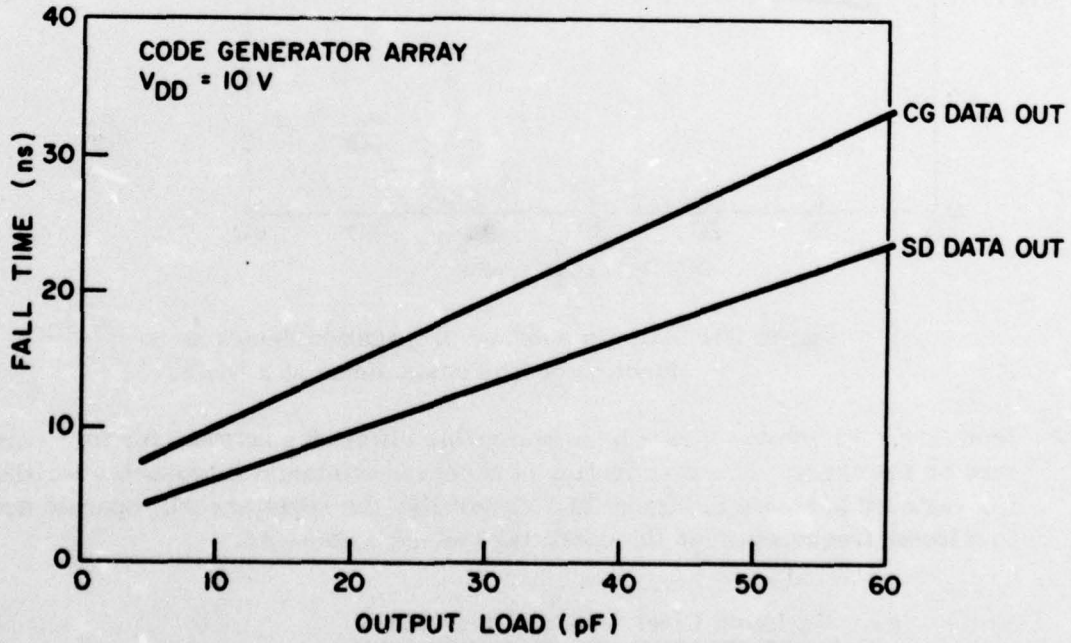


Figure 23. TCS045 average output signal fall time at 10 V.

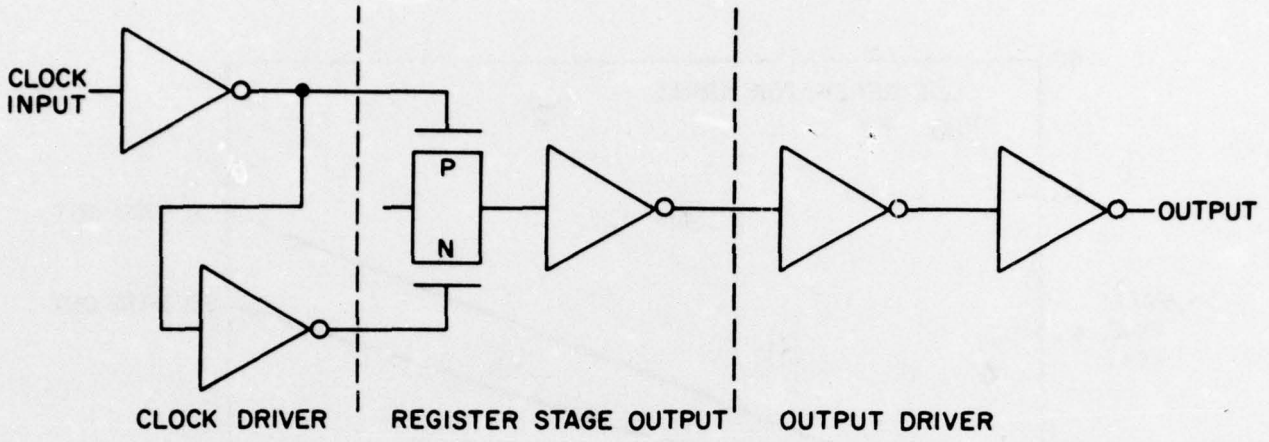


Figure 24. Code generator delay path.

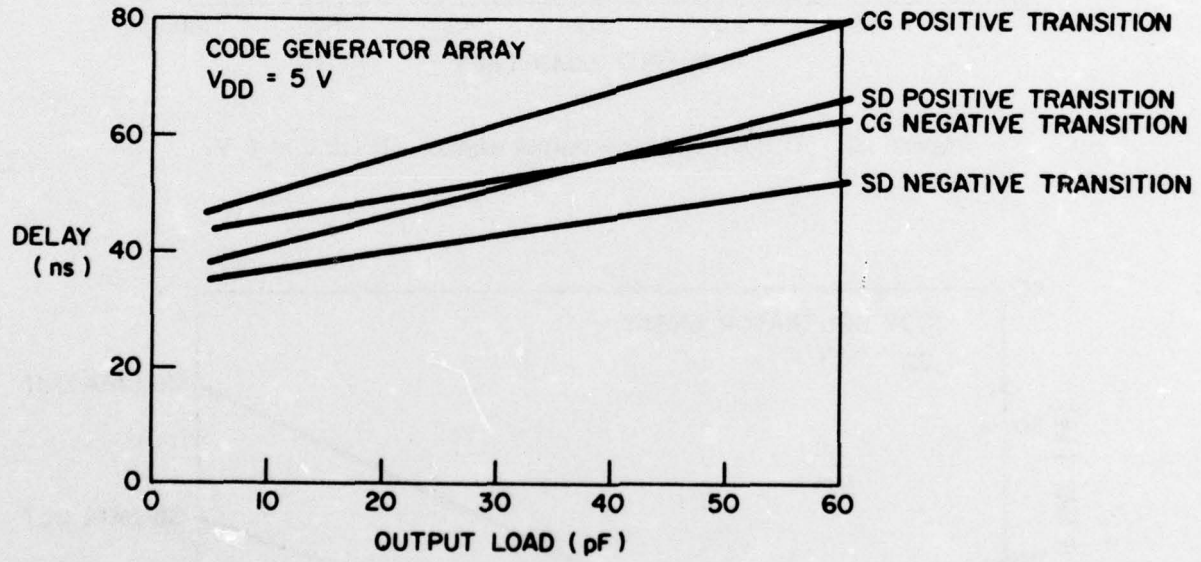


Figure 25. TCS045 average propagation delays as a function of load capacitance at 5 V.

from array to array. There is no noticeable difference between the four registers on the array. The distribution of observed minimum frequencies for the CG register is shown in Figure 27. Generally, the registers will operate down to a lower frequency when the operating voltage is reduced.

g. Maximum Clock Rise and Fall Times

The register stages used in the code generator array will fail if the input clock rise and fall times exceed some critical value. During a clock

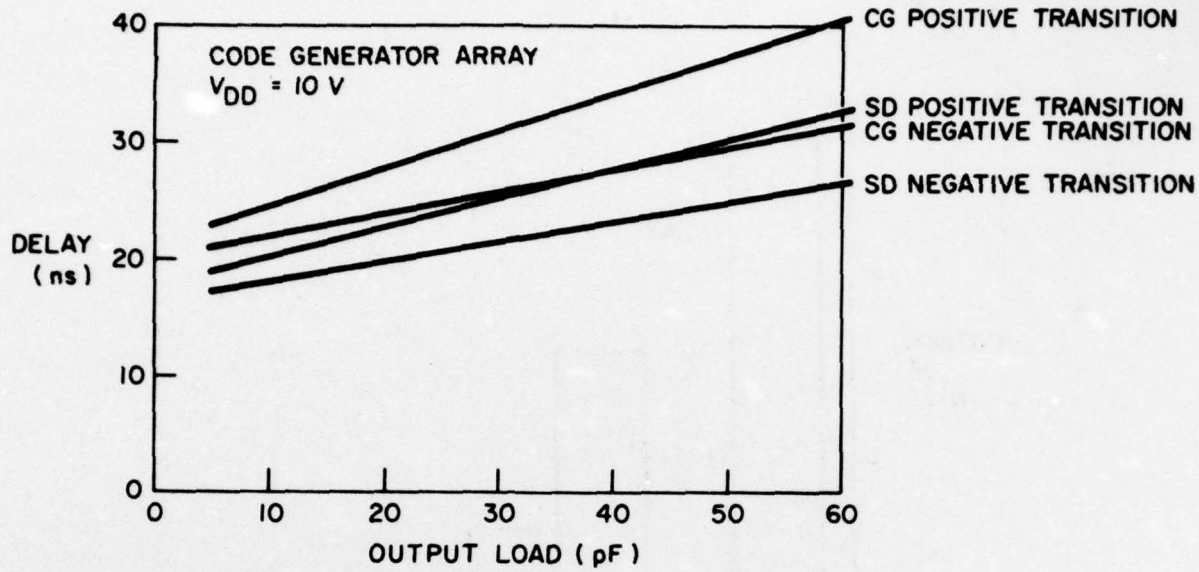
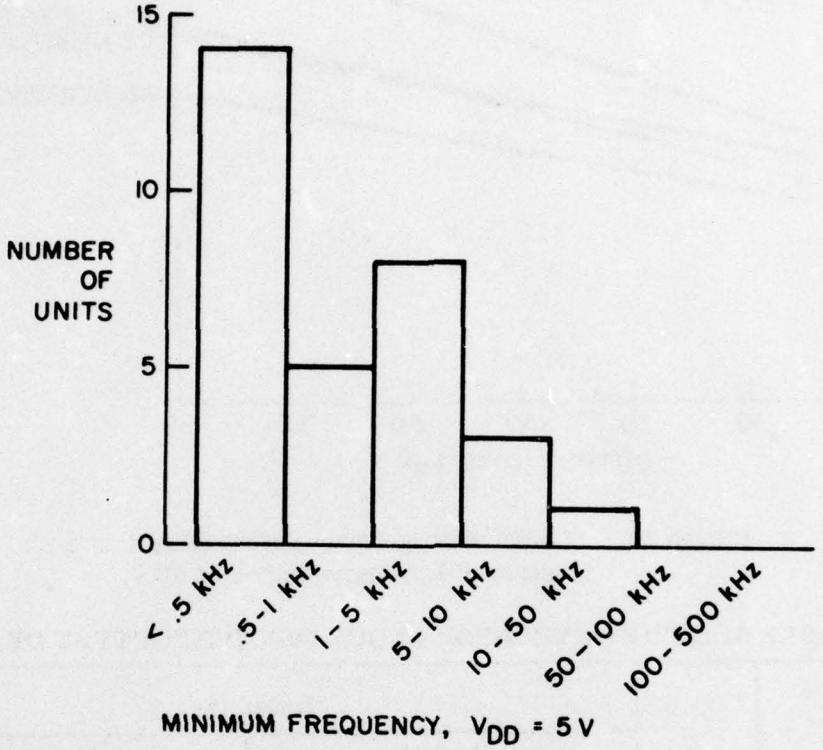


Figure 26. TCS045 average propagation delays as a function of load capacitance at 10 V.

TABLE 6. CODE GENERATOR CLOCK INPUT TO OUTPUT DELAY

Output	Load (pf)	Delay (ns)			
		At 5 V		At 10 V	
		Positive Transition	Negative Transition	Positive Transition	Negative Transition
CG Data	5	47	43	23	21
	15	53	48	27	23
	23	57	50	29	25
	38	67	55	33	27
	61	80	63	40	31
SD	5	38	35	19	17
	15	44	38	22	19
	23	47	41	23	20
	38	55	46	27	23
	61	67	52	33	26



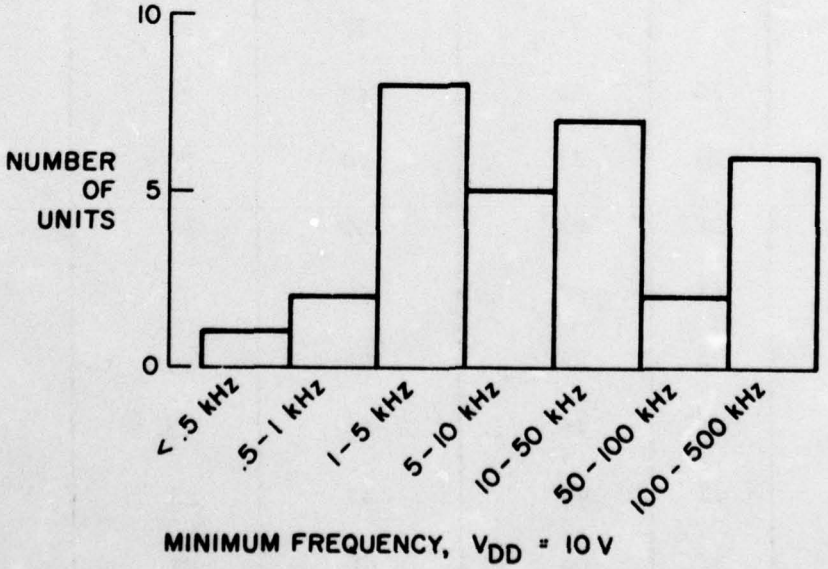


Figure 27. Distribution of observed minimum frequencies for CG register.

transition, one of the two transmission gates in the forward path is being turned on while the other is being turned off. These two transmission gates are shown in the schematic of Figure 28 as T1 and T3. Both of these transmission gates will be partly on during a clock transition. If the clock transition is too slow, a signal may propagate through both transmission gates and the intermediate logic gate before the second transmission gate is completely turned off. The use of clock drivers in the array helps to reduce the clock rise and fall times as seen at the register stages. However, if the input clock has too great a rise or fall time, the clock driver circuit will not reshape the input signal sufficiently to avoid a malfunction. The maximum input clock rise and fall times which can be tolerated decrease with increasing operating voltage since the speed of the logic increases.

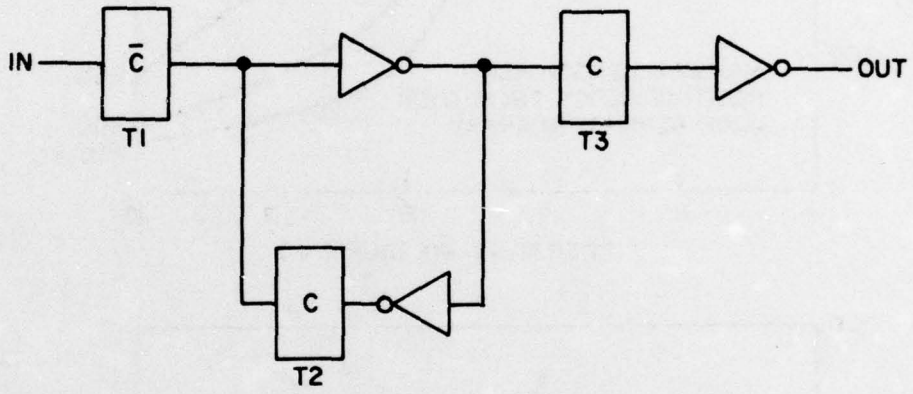
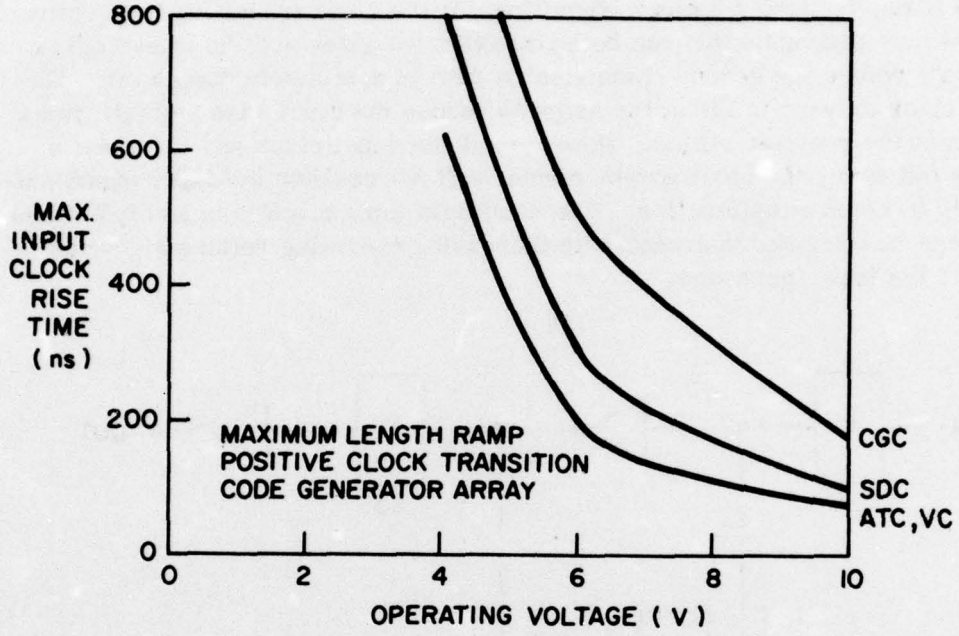


Figure 28. Typical register stage.

Typical maximum rise or fall times on the clock before failure are plotted in Figure 29. The maximum rise and fall times are obtained by applying a ramp to the clock input under test and increasing the length of the ramp until the onset of failure is reached. The rise time given is the length of the ramp. The AT and V registers which have only an inverter between the transmission gates have the lowest maximum allowable clock rise and fall times. The CG register, with the most logic between transmission gates, is the most tolerant of slow clock rise and fall times.

6. Engineering Specification

The engineering specification for the code generator array is given in Table 7. This data is a summation of test results accumulated for the code generator array.



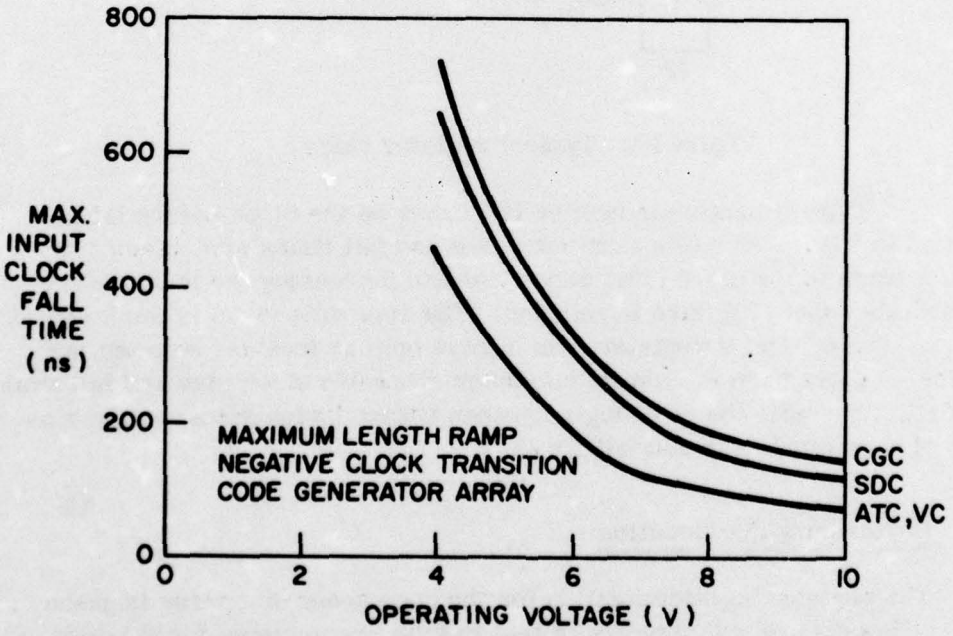


Figure 29. Typical maximum clock rise of fall times for satisfactory TCS045 operation.

TABLE 7. CODE GENERATOR ARRAY ENGINEERING SPECIFICATIONS

Parameter	Parameter Values, V_{DD} = 10 V			
	Minimum	Typical	Maximum	Units
Static V_{DD} Leakage Current		15	100	μA
Static AT V_{DD} Leakage Current		2	15	μA
Input Clock "0" State Maximum Width(1)	5	100		μs
Input Clock Rise and Fall Times(1)			70	ns
Maximum Code Generator Frequency of Operation(2)	19	22		Mbs
Maximum Code Generator Register Clock Frequency	40			MHz
Maximum V, SD, and AT Register Clock Frequency	50			MHz
CG, V, and AT Register Output Propagation Delay(3)		25	35	ns
SD Register Output Propagation Delay(3)		20	30	ns
Output Rise and Fall Times(4)		15	25	ns
Power Supply Range	3	10	15	V
Array Power Dissipation(5)		53	65	mW

NOTES:

(1) Applies to each array clock input.

(2) Generating PN sequence with 5-pF output load.

(3) Propagation delay measured from 50 percent point of signal transition relative to 50 percent point of clock signal transition with 15-pF load.

(4) Rise and fall time measurements measurements from 10 percent to 90 percent points on output signal transition with a 15-pF load.

(5) Producing a maximal length PN sequence at 10 Mbs rate. SD, V, and AT registers static. V_{DD} = 10 V.

7. Summary and Recommendations

The code generator array is a versatile building block which should have many uses in systems requiring the generation of pseudorandom sequences. Its features include fully programmable feedback taps, ability to store two separate feedback tap patterns, separate registers for initializing or reading out the contents of the code generator register, expandability to beyond the 16 stages on a single array and detection of the unity vector. Pseudorandom sequences at rates up to 10 Mbs at 5 Volts or 20 Mbs at 10 Volts are generated. Low power dissipation results from the CMOS/SOS process, typical power dissipation being 12 mW at 5 V or 53 mW at 10 V when operating at 10 Mbs.

Future design considerations should incorporate the code generator array into modules which perform the entire pseudorandom sequence generation process, including control, and which can be utilized in a system with minimum additional circuitry.

It is recommended that the Unity Vector detection circuitry be modified to allow the output from stages not being used to be excluded from the Unity Vector AND operation. This situation arises when the code generator register length is not a multiple of 16. In the present array, the outputs of all 16 stages are ANDed to produce the Unity Vector and, because of this design, an external inverter is required to provide proper operation for less than 16 stages.

B. DIGITAL ARITHMETIC SYNTHESIZERS

1. Theory of Operation

The Arithmetic Synthesizer (AS) output represents a desired output frequency signal in binary format. This signal is obtained by adding, at an adjustable clocking rate, a number, N_f, to the previously accumulated sum. If the size of this accumulator is unlimited, the magnitude of the binary number output increases without bound. However, for a finite accumulator length, the binary output magnitude overflows to a value (RES) between 0 and N_f at an average frequency f_o. F_o may be expressed as:

$$f_o = \frac{N_f}{N_c} f_c$$

where N_c is the accumulator size. This process is shown in Figure 30 and is the waveform obtained if the AS output is processed by a Digital-to-Analog Converter (DAC).

Since the overflow value (RES) is not constant, except for special cases, the output frequency, f_o, has phase and amplitude modulation. For large

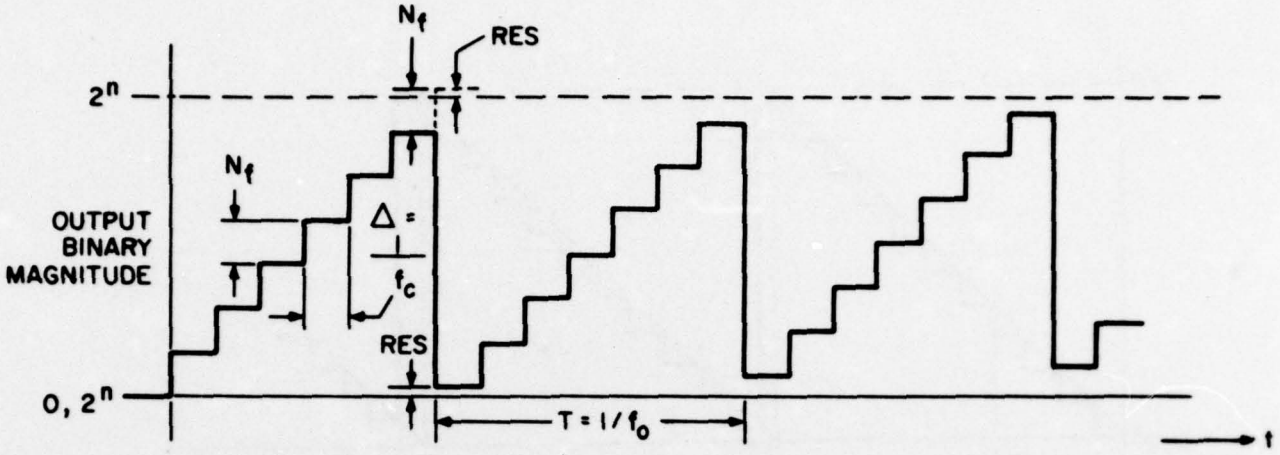


Figure 30. Arithmetic synthesizer binary output.

accumulator size (N_c), high f_c and low f_o, the modulation is small and f_o is constant and reasonably spectrally pure. Also, if the ratio f_c/f_o is an integer (2^x), then the output has very low phase noise and a minimum of spurious components, primarily $nf_c \pm mf_o$.

If one were to connect the same time point of each N_f step with a straight line beginning at 0 and reaching a maximum amplitude of 2^n before resetting to 0, the frequency of this output would be a constant f_s without phase modulation in the ideal case. This process is shown by the straight line plot in Figure 31. Thus, the binary output of each N_f step represents the amplitude of a sawtooth waveform at discrete intervals of time ($\Delta = 1/f_c$).

If the staircase signal of Figure 31 is considered the reference signal and if the sawtooth signal is considered the output of a voltage-controlled sawtooth generator, then by use of a sampling phase detector the sawtooth signal may be phase-locked to the staircase signal, resulting in an output frequency, f_s, of higher spectral purity than the frequency, f_o, of the staircase. This system is blocked out in Figure 32.

The staircase waveform of the above discussion was obtained by converting the periodically increasing binary number to a stepped analog voltage with a DAC. The sequence of the binary number format is given in Table 8 under the heading "staircase." For simplicity, the residue is assumed to be zero for each period.

If the MSB is used as one input common to a series of exclusive-OR gates and each of the remaining bits of the accumulator output is the other input to a particular exclusive-OR gate, the parallel format binary sequence at the output of the exclusive-OR gates as given in Table 8 under "triangle" is obtained. Schematically, this is shown in Figure 33.

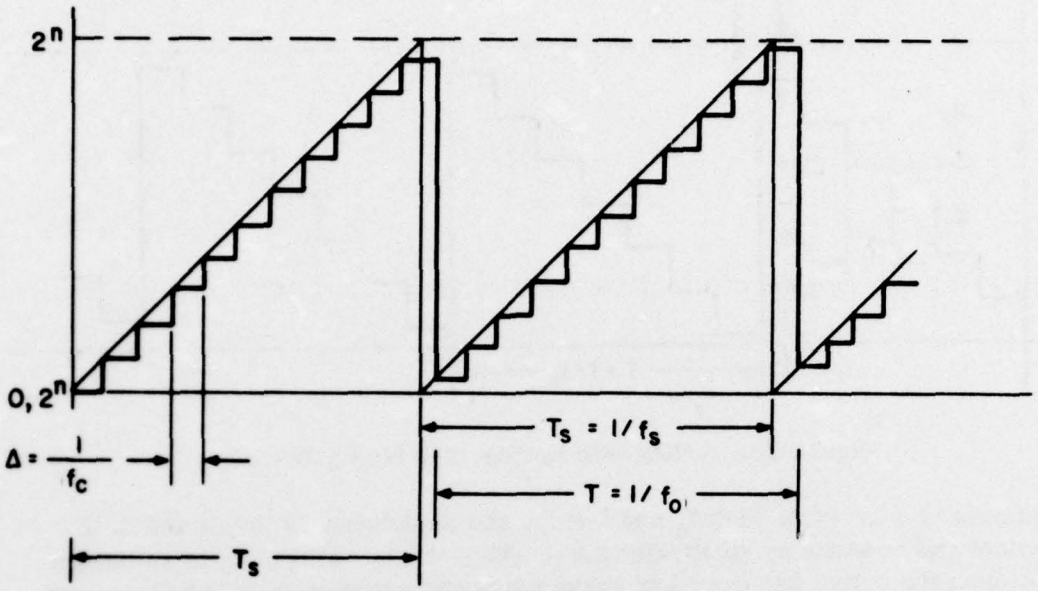


Figure 31. Generation of sawtooth.

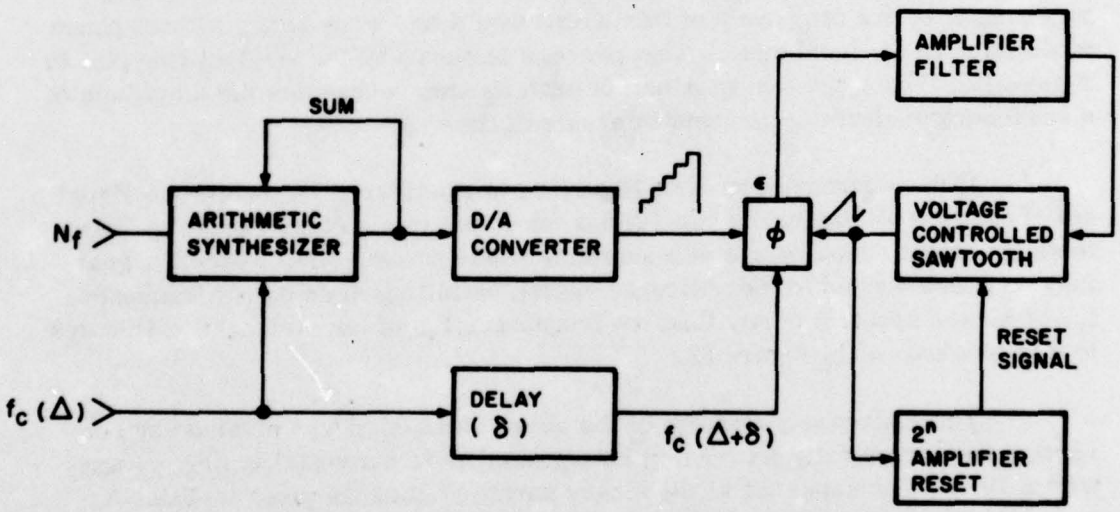


Figure 32. Arithmetic synthesizer/phase-locked loop.

Thus, by using the MSB to invert the remaining bits when the MSB is high (i.e., 1), a binary format which increases to a number "N" for one-half period then decreases to zero over the remaining one-half period is obtained. If this binary sequence is then applied to a DAC, the voltage output is the triangular waveform shown in Figure 34.. An arithmetic synthesizer using this waveform is said to be operating with a triangular wave format.

TABLE 8. BINARY FORMAT

TIME	MSB STAIRCASE LSB	MSB TRIANGLE LSB
0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0
	0 0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 1
	0 0 0 0 0 0 0 0 0 1 0	0 0 0 0 0 0 0 0 1 0
	0 0 0 0 0 0 0 0 0 1 1	0 0 0 0 0 0 0 0 1 1
	• • • • •	• • • • •
	0 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
	1 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1
	1 0 0 0 0 0 0 0 0 0 1	1 1 1 1 1 1 1 1 1 0
	1 0 0 0 0 0 0 0 0 1 0	1 1 1 1 1 1 1 1 0 1
	1 0 0 0 0 0 0 0 0 1 1	1 1 1 1 1 1 1 1 0 0
	• • • • •	• • • • •
T	1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0

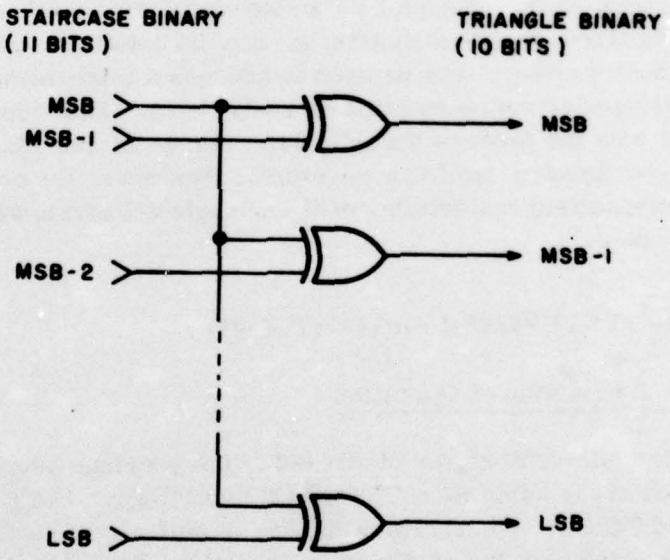


Figure 33. Staircase to triangle converter circuitry.

Although shown as a smooth curve in Figure 34, the triangular wave is a series of ascending steps followed by a series of descending steps. If the analog sawtooth VCO of Figure 32 were replaced with an analog triangle generator, the same circuit could be used to phase-lock the stepped triangular wave described above with the analog triangular wave. If phase samples were taken on the descending side, these phase samples would require a 180° phase reversal.

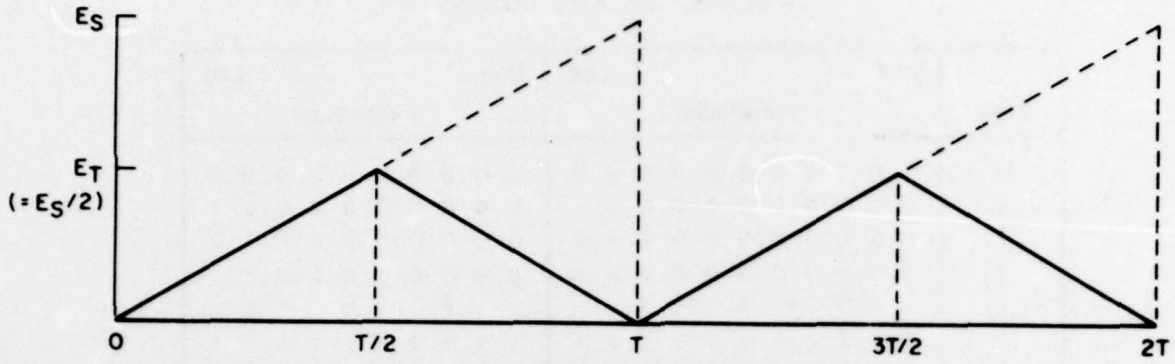


Figure 34. Triangle waveform.

Since the triangular wave is symmetrical, only even harmonics occur, suggesting that the spectrum is "purer" than the sawtooth which contains even and odd harmonics. This is indeed the case as shown later in this report when the stepped triangular output of the DAC is directly fed to the bandpass filter circuit normally used to filter the phase-locked sawtooth.

By suitable digital processing of the binary output of the AS preceding the DAC, other signal waveforms such as a sine waveform or other special waveforms, by digitized amplitude synthesis, may be obtained. For example, the stepped sawtooth waveform can be used to address a table-lookup ROM that provides a digital number representation of a sine wave. This report is concerned primarily with the process described in Figures 31 and 32, which produces a smooth, continuous, sawtooth waveform. However, for comparison purposes, performance characteristics of the triangle waveform synthesizer will also be discussed.

C. ARITHMETIC SYNTHESIZER ARRAY (TCS047)

1. General Description of Operation

The arithmetic synthesizer discussed in the previous section has been designed as an LSI array using RCA CMOS/SOS technology. The resultant array, designated TCS047, incorporates the use of self-aligned silicon gates, and has been processed with the single epitaxial silicon film $I^2(N/N)$ process.

Since the synthesizer array is essentially an arithmetic accumulator, a brief explanation of digital accumulators is in order to provide a basis of understanding for the following discussion. Figure 35 shows the logic diagram of a four-stage accumulator. The accumulator input word is simply added to the existing accumulator output word and this sum is then clocked to the output of the registers and a new cycle begins. The synthesizer chip uses this same principle except the accumulator is segmented. Figure 36 is an example of a

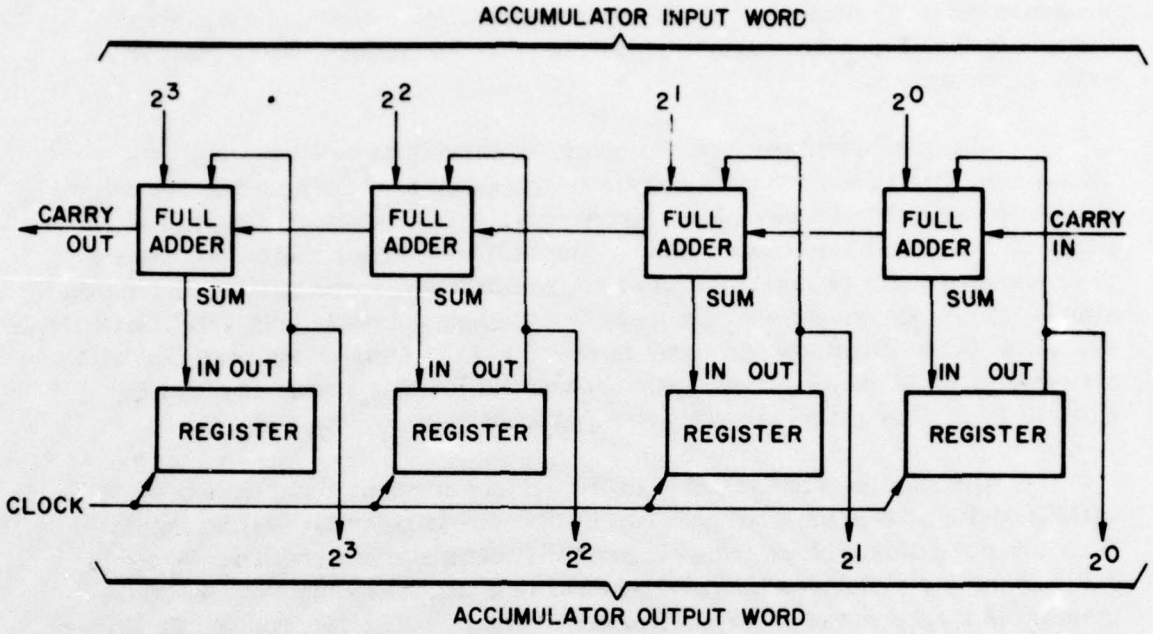


Figure 35. Four-stage accumulator.

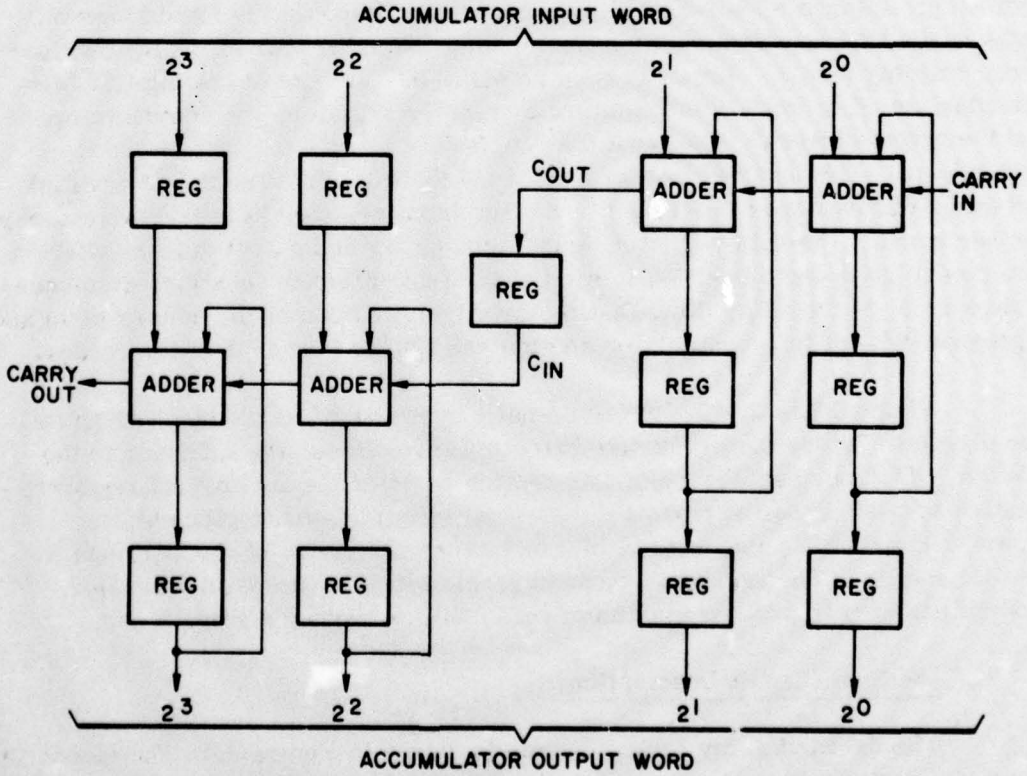


Figure 36. Segmented four-stage accumulator.

a segmented accumulator. The difference between this type and the normal version is that five extra registers are used and the output word is delayed an extra clock period.

The segmented version, however, is capable of being clocked at a higher rate than in the normal case where the speed is determined by the delay associated with four adders (three ripple carries and an output sum) and a register (setup and hold times, etc.). The segmented case has only the delay of two adders and a register. This is not a significant speed difference for this simple four-stage example as the ratio of the adder delays is only 2:1. However, the TCS047 synthesizer array is expandable to form an accumulator with a maximum of 32 stages. Each segment consists of four stages so the delay ratio is 8:1. This ratio represents a significant increase in speed.

Although the requirements of the subject contract could have been satisfied with a 20-stage accumulator, limitations in potential system applications for the building block could occur if the accumulator were limited to this size. Analysis of various potential system applications indicated that a maximum of 32 stages would ensure universal application. To incorporate 32 stages on a single array is not considered practical at this time based on array size and processing yield. To accommodate full future utilization, therefore, the 32-stage accumulator was designed so that it could be implemented by using an eight-stage segmented building block. Figure 37 is the entire logic block diagram of the 32-stage accumulator implementation using four of the synthesizer array building blocks. Each array is an eight-bit segment of the total 32 bits and consists of an input data register, a transfer register, the accumulator, and the output drivers. The input data register receives the input word in serial form. The transfer register converts the word from serial to parallel and temporarily stores the input word. The input register is then free to accept another word. The data register, transfer register and output drivers share a common relative logic position in each of the four different locations or modes (0 through 3) of the chip. Note that the relative positions of the adders (A's) and registers (R's) of the accumulator section are different in each of the modes.

Figure 38 is the TCS047 arithmetic synthesizer array block diagram. The diagram divides the array into two similar sections, the 4 LSBs and the 4 MSBs. The four switches (S's) per section position the adders and registers relative to one another to permit the 32-stage accumulator implementation shown in Figure 37. Two control bits determine the status of the switches for the four modes. The array has three separate clock inputs (data, transfer, and synthesizer) to provide maximum versatility for array applications.

2. Detailed Circuit Description

The detailed array logic diagram is shown in Figure 39. The blocks in Figure 39 designated R correspond to the data and accumulator registers and

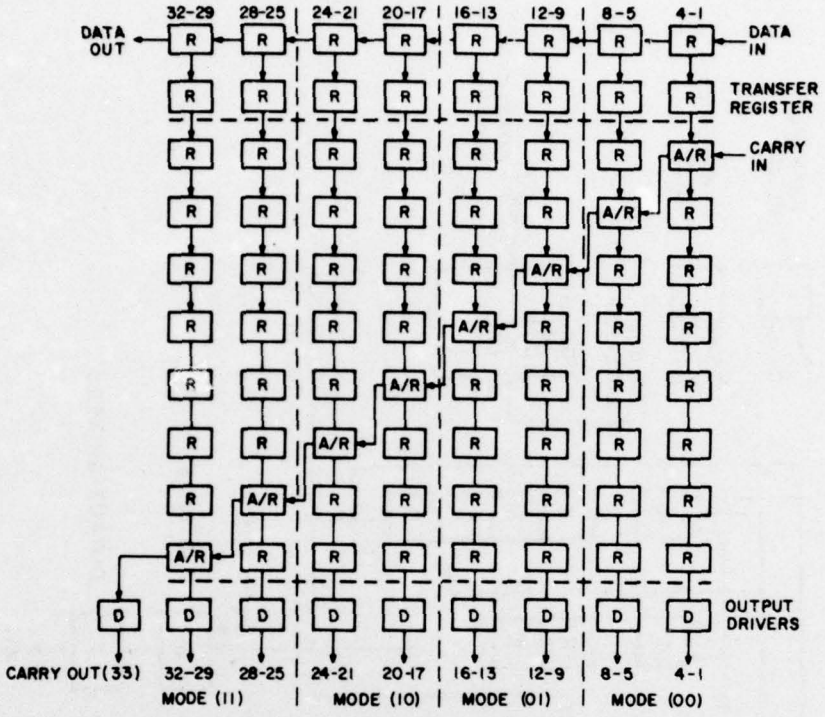


Figure 37. Logic block diagram of 32-stage accumulator.

T-R designates the transfer registers. The block labeled P is an input protection device. The blocks identified as input/output switches are comprised mainly of transmission gates and are shown as a buffer with an additional input. The transmission gate is enabled when the additional input is a "1". The remainder of the logic is in standard form.

The signal nomenclature should be explained for the purpose of clarity. The LSB section has a set of four registers, labeled 4R, a two-register set (2R), and an adder followed by two registers (ARR). The MSB has the same 4R and 2R sets and a register-adder-register (RAR) set. These logic chains can also be found in Figures 37 and 38, which should be of help in understanding the detailed logic.

For those who might want to pick out individual logic elements on an actual chip, the topography of the logic shown in the photomicrograph of the array, Figure 40, closely follows the logic topography in Figure 39.

The logic diagrams and the number of devices used in the basic circuits of this array are shown in Figure 41. The data and accumulator registers, Figure 42, are quasi-static types. In this circuit, the clock (C) and clock ($\overline{C}$) signals are complements of each other. During the $\overline{C}$ portion of a clock cycle ($\overline{C}$ is a "1"), the $\overline{C}$ transmission gate (T-gate) is on and the C T-gates are off. The input

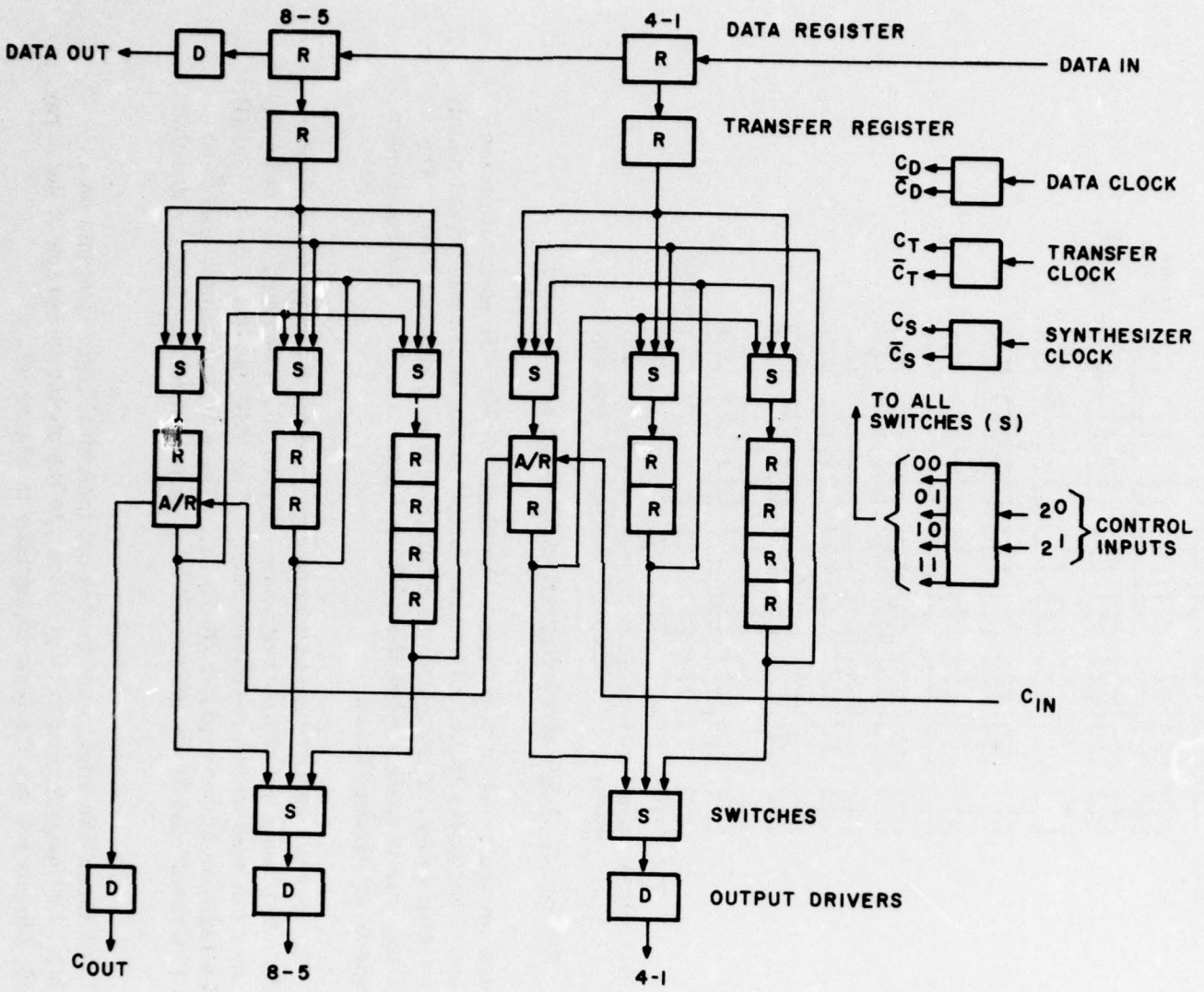
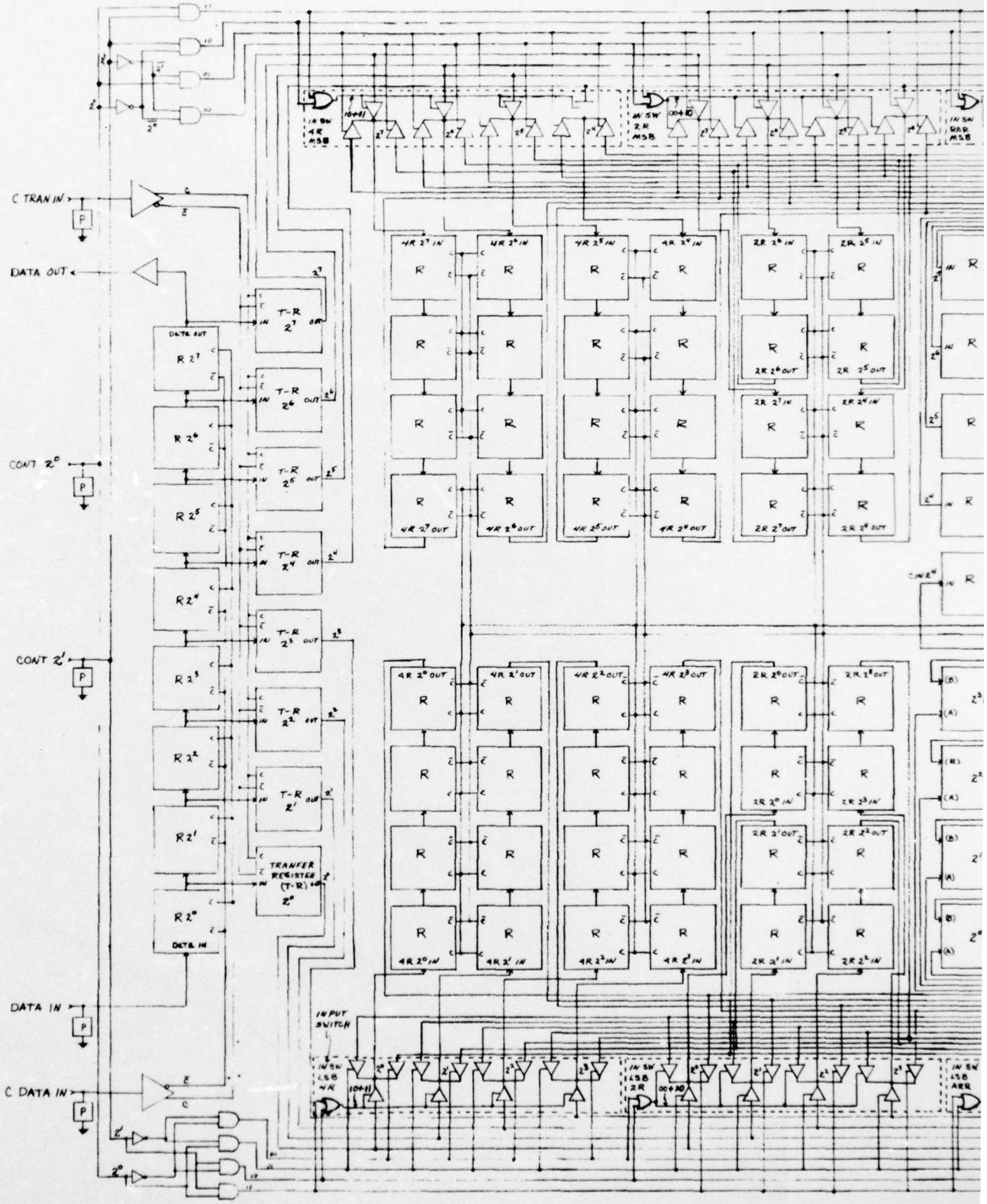


Figure 38. Block diagram of TCS047 arithmetic synthesizer array.



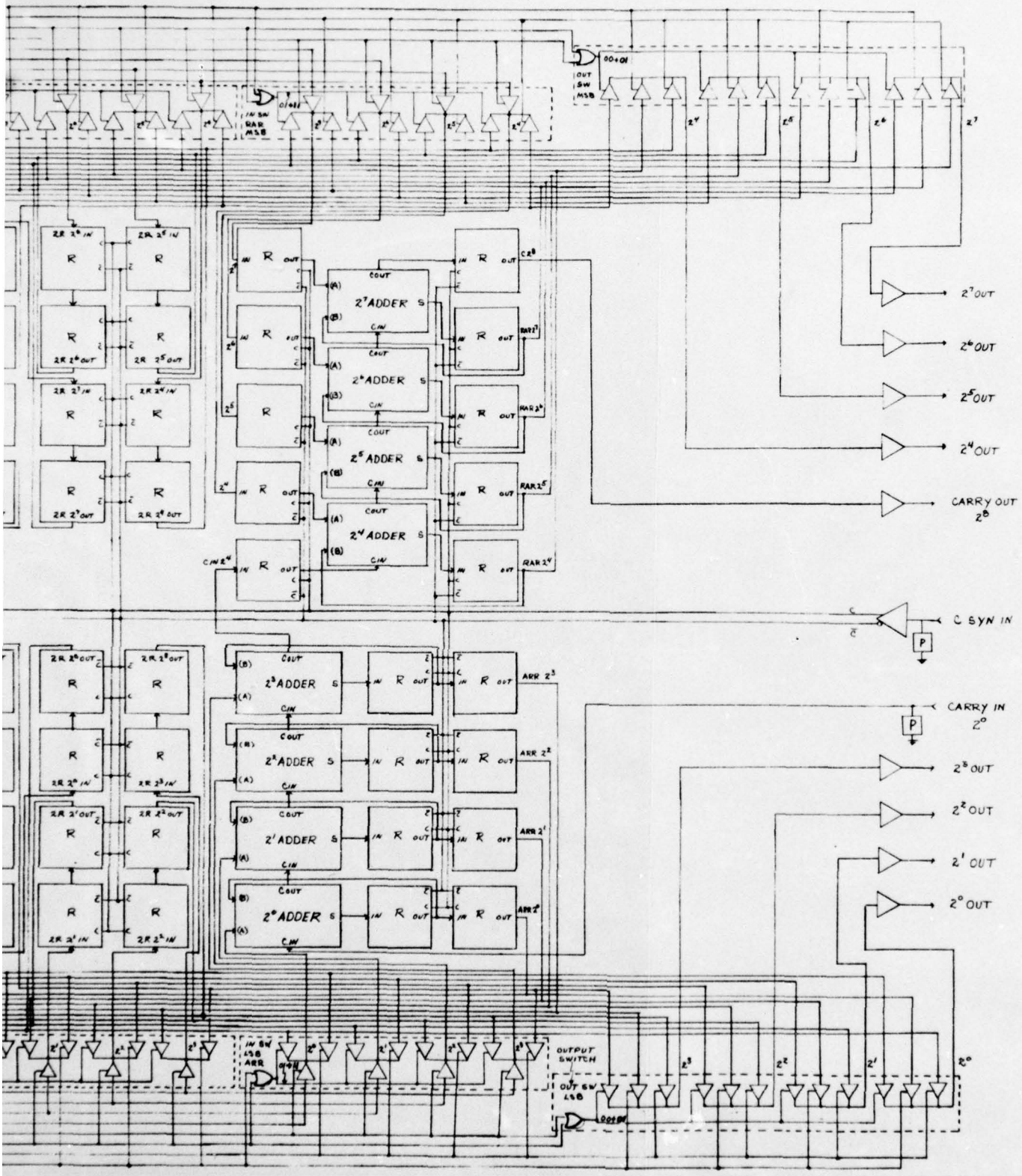


Figure 39. Detailed logic diagram of synthesizer array.

2

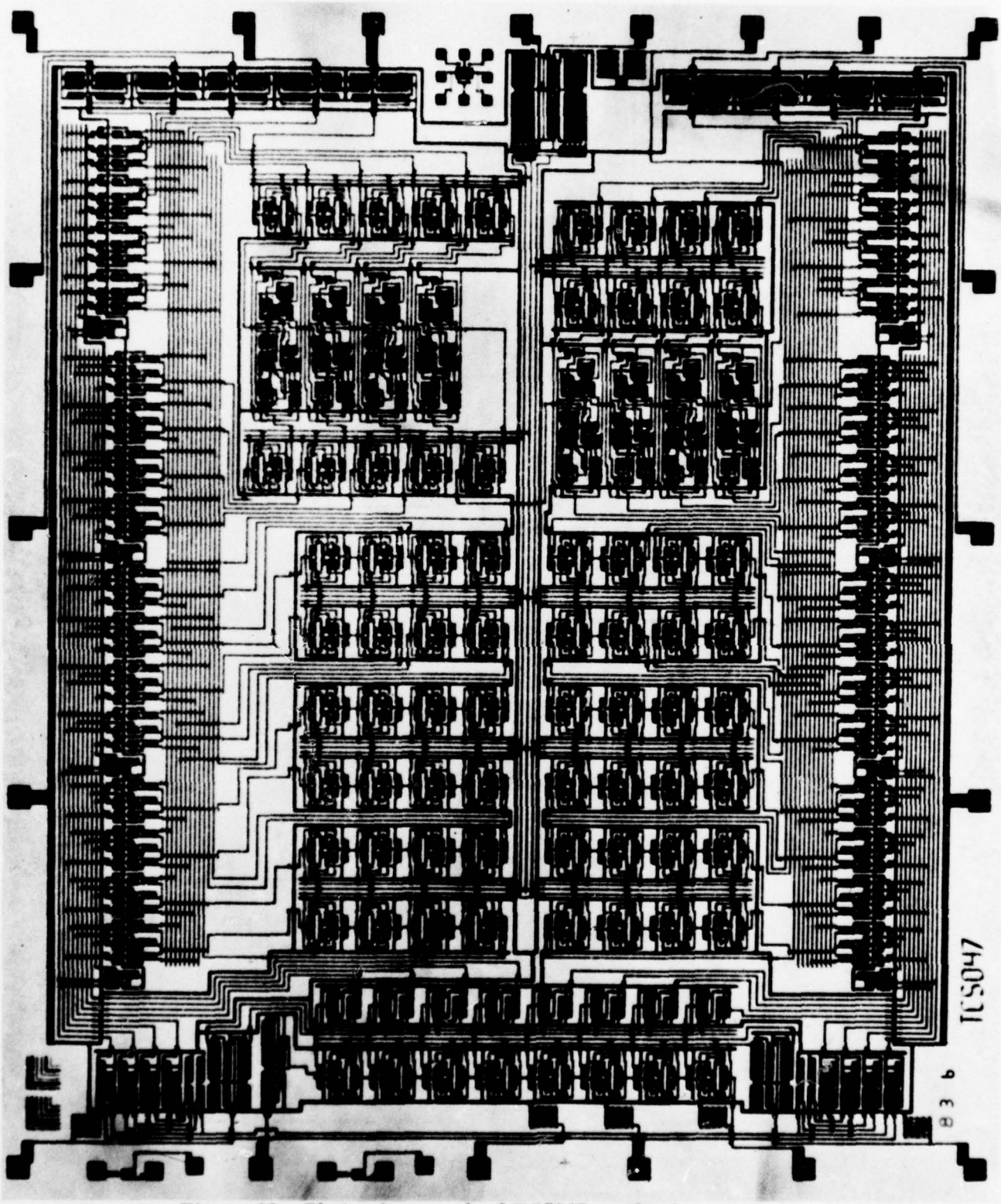


Figure 40. Photomicrograph of TCS047 synthesizer array.

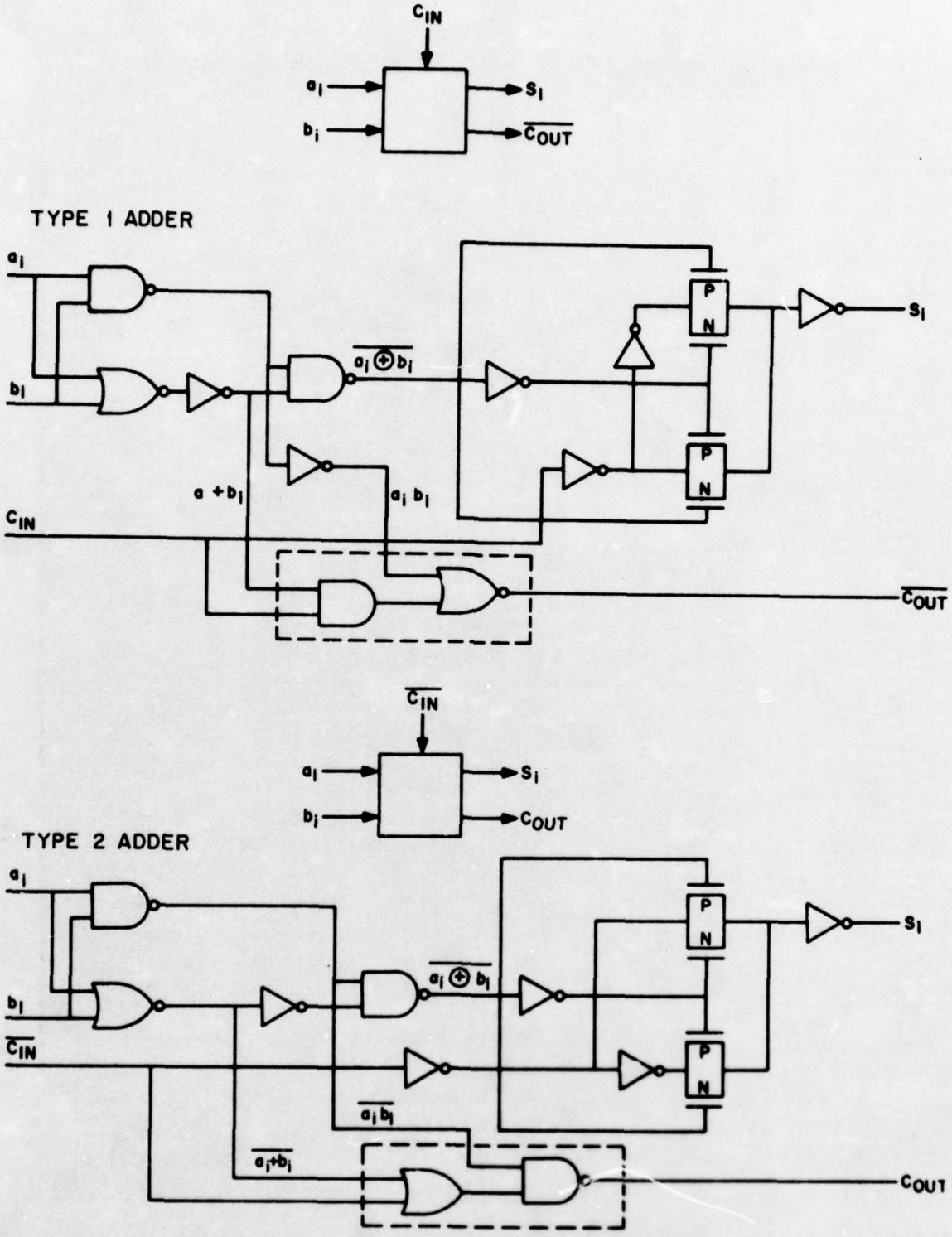


Figure 41. Logic diagrams for TCS047 adder circuits.

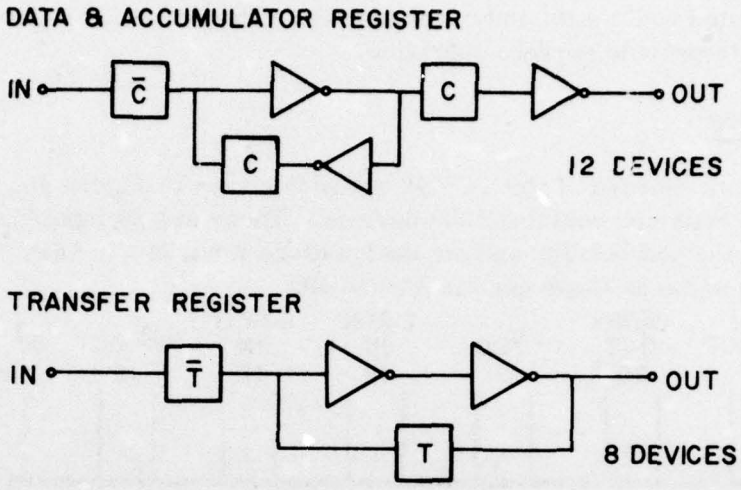


Figure 42. Data, accumulator and transfer shift register logic diagrams.

state is sampled and fed into the first two inverters. The output inverter state is held by the storage of the voltage on the inverter gate capacitance. The leakage current through the off T-gate limits the time duration of the $\overline{C}$ portion of the clock cycle.

The C T-gates are on and the $\overline{C}$ T-gates are off during the C portion of the clock cycle. The input is inhibited and the first two inverters become cross coupled. The input state originally sampled during the $\overline{C}$ period, is fed to the output of the last inverter. The status of the register can be held indefinitely as long as C is a 1 because none of the gates is left floating and the input inverters are cross coupled. The quasi-static register is used instead of the fully static register in the interest of speed, power, and size.

The transfer register, Figure 42, is a slight variation of the data and accumulator register. The input is sampled when the transfer clock ($\overline{TC}$) signal is a 1. The input state is immediately transferred to the output. This state is held when TC is a 1. The register is stable for any 1 duration of either TC or $\overline{TC}$ and as such, it is a fully static register.

The primary concern, when a block of four adders is considered, is to minimize the carry ripple delay as this path represents the worst-case delay. Two adder circuits are used to accomplish the minimization and are shown in Figure 41. The carry delay is the delay of an AND/NOR gate or an OR/NAND gate. These two types of logic elements are considered a single complex gate that constitutes a single level of logic. This arrangement minimizes the carry delay as opposed to a multilevel logic arrangement. The a and b inputs, normally present before the carry input, are added modulo-2 and used to prime the

T-gates in the sum channel. The complex gate in the carry channel is also primed by the a and b inputs. Therefore, when the carry signal arrives, the carry state is quickly translated to the sum and carry outputs. The two adder types are alternately used to provide correct operation.

3. Packaging

A photomicrograph of the TCS047 array is shown in Figure 40. The array size is 178 x 214 mils and contains 1938 devices. There are 20 input/output pads. Figure 43 shows the pad bonding and pin designations for a 24-pin DIP. The designations are the same as those used in Figure 39.

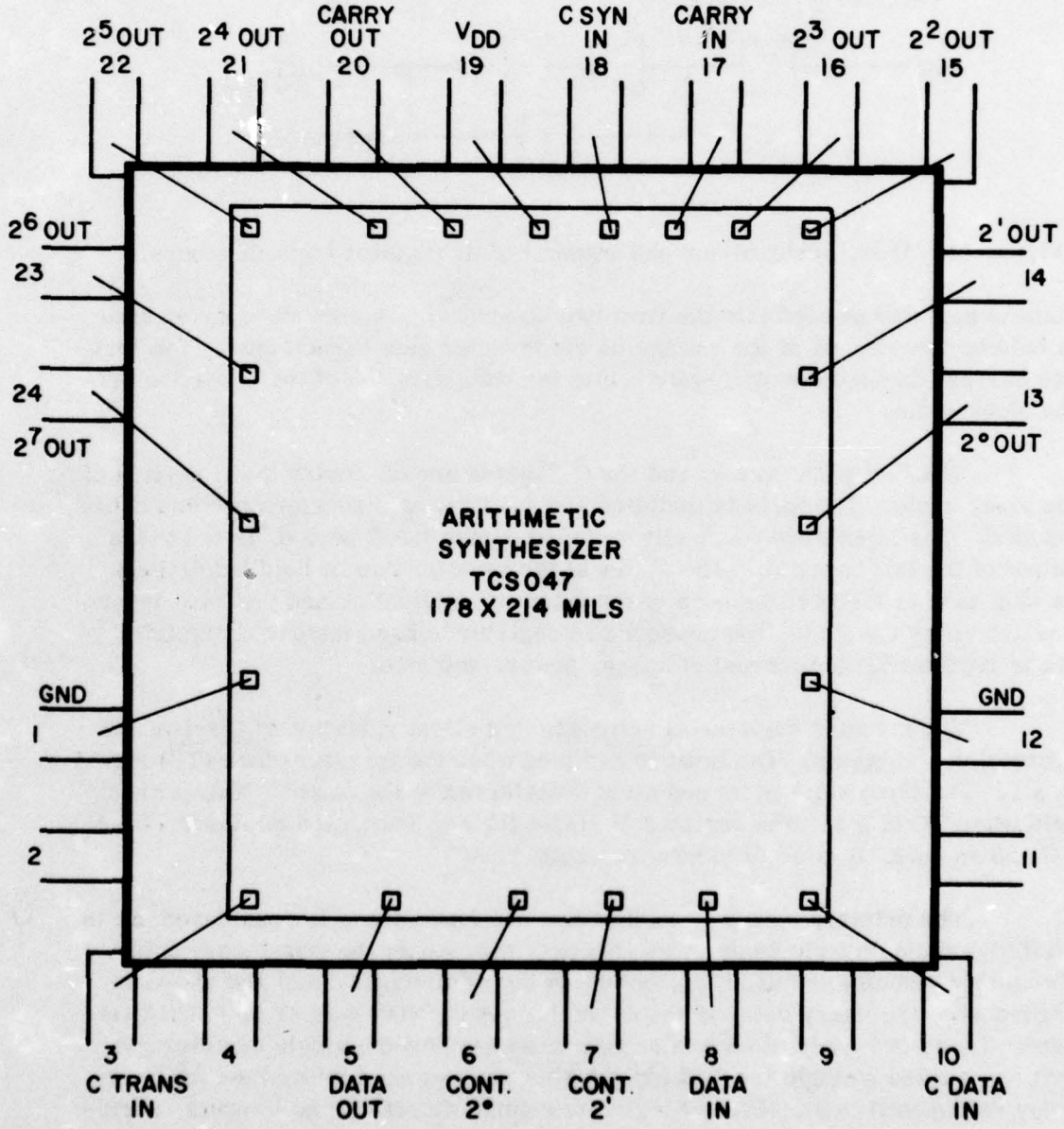


Figure 43. Pad bonding and pin designations for a 24-pin DIP.

4. Performance Characteristics

a. Test Philosophy

Testing of the TCS047 Synthesizer array was divided into two phases. The initial phase is represented by the low frequency (50 kb/s) wafer probe dynamic test. Here, a test sequence was developed consisting of 176 input words, or combinations, that was designed to exercise all the inputs to the various circuits, such as registers, address, and switches on the array. Each circuit input is exercised in both the 1 and 0 states. Once the array passes this test, the die is packaged, retested against the same sequence, and then given various performance characteristic tests such as high speed operation, power dissipation, and leakage current measurement, all as a function of voltage.

Since the array does not have an accumulator reset facility a special initializing sequence is required prior to the start of any test sequence. The LSB of the accumulator is added to itself which sequentially clears the circuit by manipulating the 2^0 and 2^1 control bits. During this reset operation, the data register is dynamically checked. With a known accumulator state and input word, the remainder of the logic is then tested by the input test word sequence.

b. Test Results

The following test results are based on the testing of 40 units. The units were fabricated using the standard $I^2(N/N)$ process with a gate length (mask dimension) of 0.25 mil.

Figure 44 is a curve of the typical leakage characteristics. The leakage measurements are taken with the clock inputs in the 1 state and all other inputs in the 0 state.

The array speed-power curves are shown in Figure 45 in addition to the power, these curves also show the maximum operating frequencies for the corresponding supply voltages (V_{DD}). Normally, average power is plotted in these curves but in this case maximum power is plotted. The reason for this is that the array power is a function of the input data word and the range of these words with their corresponding powers is large. Also, the test condition for maximum power is the most rigorous test of the logic. This condition also provides the most valid value for the array's maximum frequency of operation. All the registers are operating at the same frequency during this test. It is estimated that the average power for the array is between 30 percent and 50 percent of the values shown in the curves. Average power is difficult to estimate as it is very dependent upon the particular application, input word size and clocking frequency.

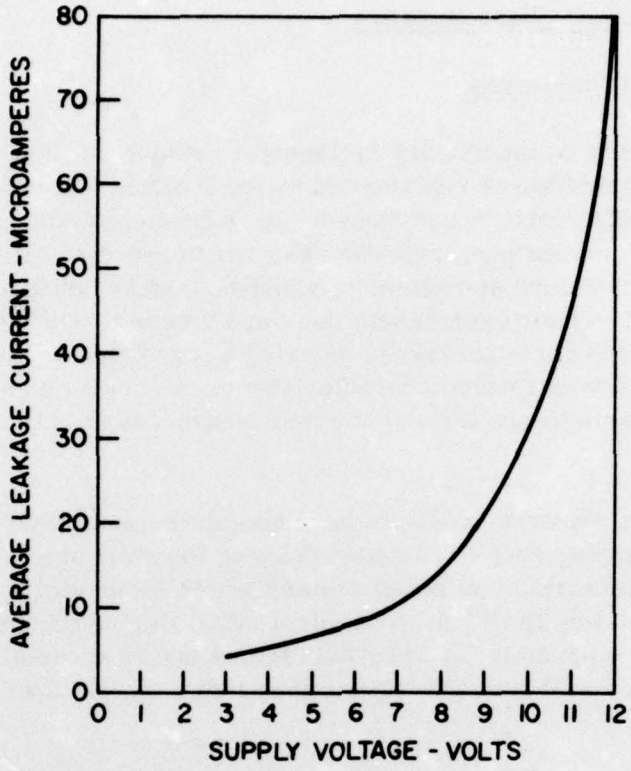


Figure 44. TCS047 typical leakage characteristics.

Table 9 contains the clock and data input signal characteristics and Table 10 contains the output signal response characteristics. There are essentially three types of output signals; 2^n output (any of the 8 accumulator outputs), the carry out, and the data out. The information is given for various supply voltages and capacitive loads. The signal propagation delay measurements were taken relative to the corresponding input clock signal. The delays of the internal clock driver circuits are thus included in the delay measurements. The accumulator outputs have the longest delays as these signals pass through the additional delay of the output switch circuits.

c. Engineering Specification

The engineering specification for the array is contained in Table 11. This is an accumulation of the previously discussed typical test results with the addition of minimum and maximum values.

5. Applications

General uses of the chip, rather than specific applications, and the relationship of the factors that determine the synthesizer output frequencies will be discussed in this section.

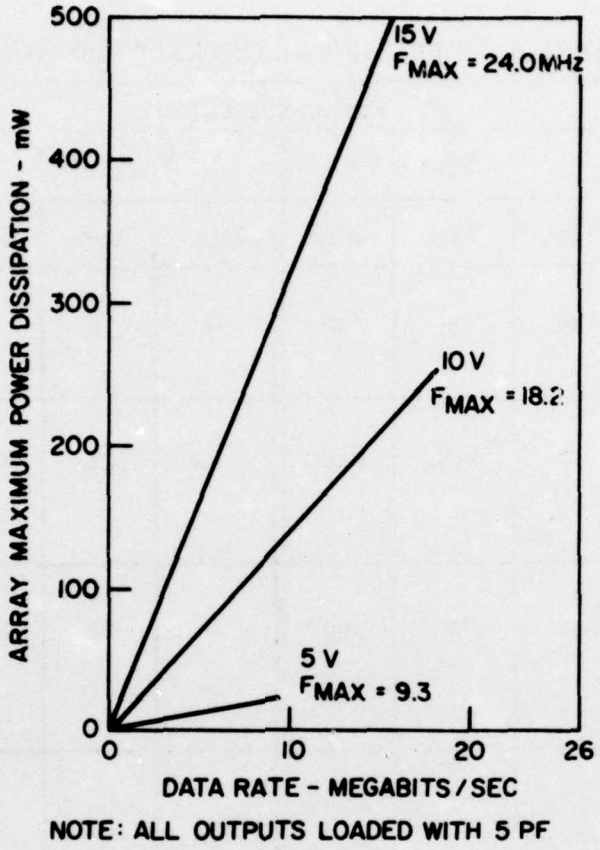


Figure 45. Speed-power curves for TCS047 array.

The accumulator output value has a positive slope. If the output were connected to a D/A converter, the D/A output would be a sawtooth (staircase) signal with the increment of each of the stairs equal to the value of the input word in the transfer register. Periodically, the accumulator overflows and the reset value or residue, is always less than the value of the input word.

The relationship between the average sawtooth output frequency and the other chip factors is given by the following equation:

$$f_o = \frac{f_s (W)}{2^N} \qquad (1)$$

where f_o = Average sawtooth output frequency

f_s = Synthesizer clock frequency

W = Value of the input word

N = Number of accumulator stages

TABLE 9. INPUT SIGNAL CHARACTERISTICS

Parameters	Parameter Values					
	V_{DD} = 5 V			V_{DD} = 10 V		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Clock 0 State Minimum Width T_C - 0 Min. (ns)	30	36	40	8	10	12
Clock 0 State Maximum Width T_C - 0 Max.(2) (μs)	83	218	1500	50	125	450
Clock Rise & Fall Times T_{C-R} & T_{C-F}(2) (ns)	260	363	600	50	84	130
Minimum Input Clock to Data in Delay $T_{C-D_{IN}}$ (ns)	5.5	6	8	8.5	10	11

(1) Clock refers to data, transfer, and synthesizer clocks waveforms.

(2) Clock refers to data & synthesizer clock waveforms.

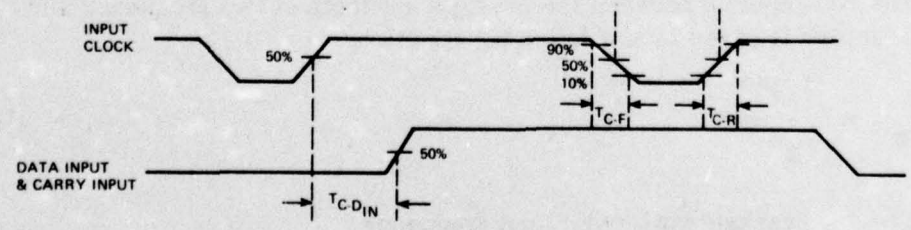


TABLE 10. OUTPUT SIGNAL CHARACTERISTICS

Parameters		Parameter Values					
		V_{DD} = 5 V			V_{DD} = 10 V		
		Min.	Typ.	Max.	Min.	Typ.	Max.
Synthesizer Maximum Frequency of Operation (MHz)		6.9	9.3	11.8	14.5	18.2	22.1
	Load (pF)						
2^n Output Propagation Delay (1) (ns)	5	60	74	92	33	37	45
	15	68	83	104	37	42	49
	25	75	90	114	39	46	54
Carry Out Propagation Delay(1)(ns)	5	40	49	58	22	26	28
	15	48	58	70	26	30	34
	25	55	65	78	29	34	38
Data Out Propagation Delay(1) (ns)	5	34	45	62	19	24	31
	15	42	55	72	23	29	38
	25	48	63	81	28	33	43
2^n Output Rise Time(2) (ns)	5	22	29	40	14	15	19
	15	34	47	70	23	26	31
	25	48	66	92	32	36	42
Carry Out Rise Time(2) (ns)	5	20	25	50	11	13	15
	15	30	41	66	18	22	26
	25	46	59	84	26	31	37
Data Out Rise Time(2) (ns)	5	22	27	36	11	15	17
	15	36	47	66	20	25	34
	25	48	68	96	29	35	47
2^n Output Fall Time(2) (ns)	5	18	25	54	11	14	17
	15	30	38	52	17	22	27
	25	38	52	68	24	30	47
Carry Out Fall Time(2) (ns)	5	16	20	32	9	10	12
	15	24	32	46	15	18	23
	25	36	46	60	23	26	31
Data Out Fall Time(2) (ns)	5	16	23	48	9	12	24
	15	26	38	70	16	21	38
	25	36	54	110	20	29	50

(1) Propagation delay measured from 50% point on output signal relative to 50% on input clock signal.

(2) Rise and fall times measured from 10% to 90% points on output signal transitions.

TABLE 11. TCS047 SYNTHESIZER ARRAY ENGINEERING SPECIFICATION

Parameter	Parameter Values @ V_{DD} = 10 V	
	Minimum	Maximum
Static Leakage Current [2] (μA)		100
Input Clock "0" State Minimum Width[2] $T_{C-0\ min}$ (ns)		15
Input Clock "0" State Maximum Width[2] $T_{C-0\ max}$ (μs)	30	
Input Clock Rise & Fall Times[2] T_{C-R} & T_{C-F} (ns)		100
Input Clock to Data In Delay T_{C-DIN} (ns)	15	
Synthesizer Frequency of Operation (MHz)	14	
2^n Output Propagation Delay[3] (ns)		55
Carry Out Propagation Delay[3] (ns)		40
Data Propagation Delay[3] (ns)		45
2^n Output Rise & Fall Times[4] (ns)		35
Carry Out Rise & Fall Times[4] (ns)		30
Data Out Rise & Fall Times[4] (ns)		40
Power Supply Range of Operation (V)	3	15
Array Power Dissipation @ 10 MHz with 15-pF loads (mW)		250

(1) Measurements made with all clock inputs 1 and all other inputs 0.
(2) Clock refers to data, transfer, and synthesizer input clock waveforms.
(3) Propagation delay measured from 50% point on signal transition relative to 50% point on clock signal transition.
(4) Rise and fall time measurements measured from 10% to 90% points on output signal transitions with a 15-pF load.

The minimum change in the output frequency (min Δf_o) or frequency spacing occurs when the input word changes by one ($\Delta W = 1$). Substitution in equation 1 produces the desired relationship:

$$\min \Delta f_o = \frac{f_s}{2^N} \tag{2}$$

Another way to look at frequency spacing is in terms of resolution. Given a desired output frequency, within what tolerance can the synthesizer resolve this frequency?

$$\text{Resolution} = \pm\frac{1}{2} \min \Delta f_o = \pm \frac{f_s}{2^{N+1}} \tag{3}$$

In normal operation, the periods of the sawtooth waves will vary along with the maximum and reset values of the accumulator as shown in Figure 31. These variations result in both phase and amplitude modulation of the desired output frequency, f_o. Synchronous conditions do exist where these variations are completely eliminated. This occurs when the accumulator values during a cycle are exactly repeated in subsequent cycles. This occurs only when

$$W = 2^j \qquad j = 0, 1, 2 \ldots N$$

Rearranging Equation 1 and substituting this value of W results in the following ratio of f_s/f_o for synchronous operation:

$$f_s/f_o = \frac{2^N}{2^j} = k \qquad k = 2^N, 2^{N-1}, \ldots 4, 2, 1 \tag{4}$$

Equations 1 through 4 cover the basic relationships between the arithmetic synthesizer array factors. The quality of the output spectrum and general uses will now be covered.

Figure 46 shows two basic system configurations. The simplest is the direct type, Figure 46A, where the accumulator digital word is converted to an analog signal and then passed through a bandpass filter (BPF). In the cleanup loop type, the conversion is again made to an analog signal but here the voltage is then used as a reference signal to which the internally generated analog sawtooth is phase locked. The internal sawtooth signal is then filtered by the BPF.

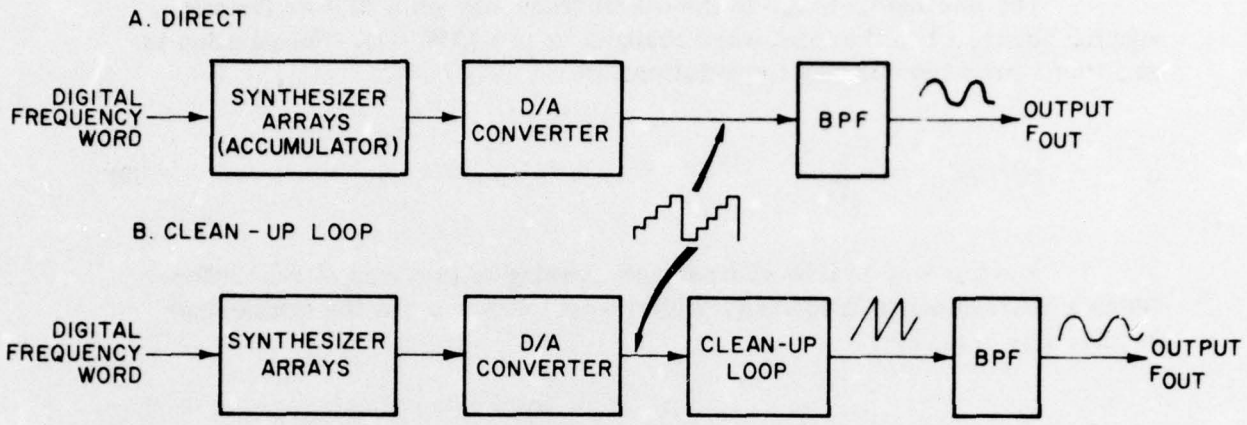


Figure 46. System block diagrams for arithmetic synthesizers.

The harmonic content of a sawtooth wave is shown in Equation 5:

$$\text{Sawtooth } f(t) = \frac{2}{\pi} \Sigma(-1)^{n-1} \frac{1}{n} \sin n\omega t \qquad (5)$$

where n = integer.

The amplitudes of the second and third harmonics relative to the fundamental are down only 6 dB and 10 dB, respectively. The sawtooth operation is therefore limited to applications where the ratio of the output frequencies f_{max}/f_{min}, is less than two. This allows a filter on the output to reduce the second and third harmonics of f_{min} sufficiently such that the output will be a reasonably clean sinusoid.

The phase and amplitude modulation caused by the nonsynchronous condition of the accumulator was previously mentioned. This modulation can be minimized in two different ways.

First, the synthesizer clock rate (f_s) and the number of accumulator stages (N) should be as high as possible. This increases the number of steps per sawtooth cycle and decreases the size of each step. The phase error is reduced by the greater number of steps per cycle and the amplitude variations are reduced by the reduced size of each step.

The D/A converter is usually the limiting factor in the system. It generally limits the clocking rate (f_s) and it has an inherent SNR which is dependent on the number of input bits of the D/A.

A second method of using the TCS047 synthesizer array is to incorporate the use of a cleanup loop as shown in Figure 46B. The internally generated

sawtooth always starts (reset value) at the same value and ends at the same value thereby eliminating the amplitude variation. The internal sawtooth can be locked to the reference signal by sampling the two signals when the reference signal is in the vicinity of the middle of its positive going staircase. The reference signal is always at the correct value at this time if it were compared to a perfect sawtooth waveform. This disregards the quantization error caused by the limited number of bits in the accumulator and the D/A converter. At any rate, the internally generated sawtooth wave does not have the phase noise that is associated with the reference waveform. More will be discussed about this method in the following sections as this is the method used to develop the synthesizer module.

The synthesizer output can be easily converted from a sawtooth wave to a triangular wave. The conversion consists of complementing (inverting) the synthesizer output word on alternate sawtooth cycles. In the actual implementation of this conversion, the MSB of the output word is used as the control signal to the complementing logic. This in effect reduces the number of accumulator stages by one as the MSB is no longer used as an output bit. Therefore in Equations 1 through 4, the variable N is replaced by N-1. This is valid when the triangle wave replaces the sawtooth wave in the systems shown in Figure 46.

The harmonic content of a triangle wave is shown in Equation 6:

$$\text{Triangle } f(t) = \frac{8}{\pi^2} \sum (-1)^{\frac{n-1}{2}} \left(\frac{1}{n^2} \sin n\omega t \right) \tag{6}$$

where n = odd integers.

The even harmonics are essentially eliminated and the third harmonic is about 20 dB down relative to the fundamental. The use of the triangle wave in the system in Figure 46 is thus limited to an output frequency band where f_{max}/f_{min} is less than three. The ratio of f_{max}/f_{min} can be increased by including a ROM in the system. The ROM converts the triangle wave to a sine wave. The block diagrams of two systems that use the ROMs are shown in Figure 47. Example waveforms associated with the two systems are shown in Figure 48 to clarify the operation. It should be noted in the system using the 90° ROM that the effective number of accumulator stages has again been decreased by one. Therefore, in Equations 1 through 4, the variable N is replaced by N-2. The only difference in the two systems is in the ROMs. Assuming the ROMs are the same size, the 90° ROM phase and amplitude resolution is greater by a factor of two. The spectral purity desired in the output signal will dictate which type ROM system must be used.

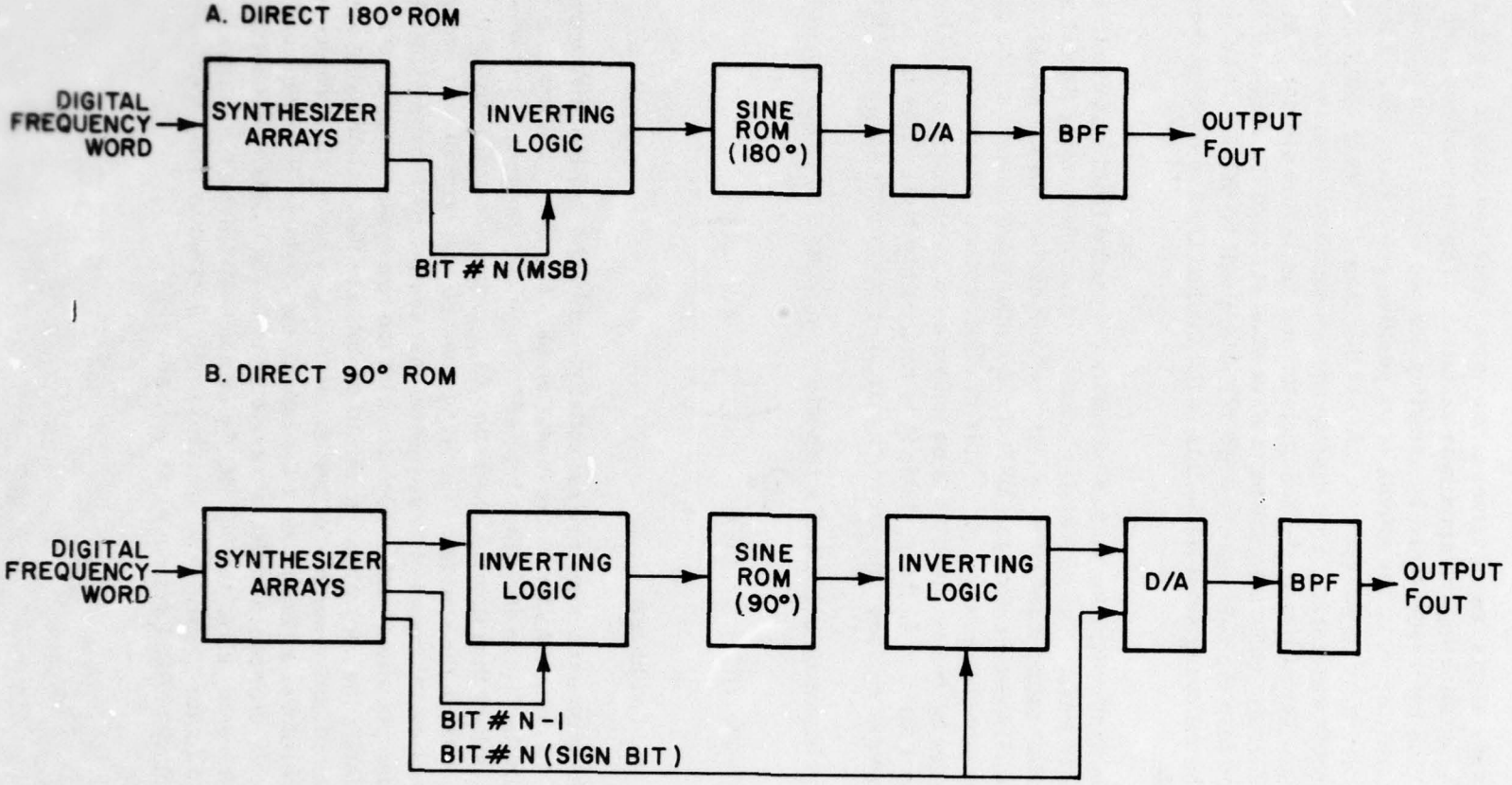


Figure 47. System block diagrams for arithmetic synthesizers using ROMs.

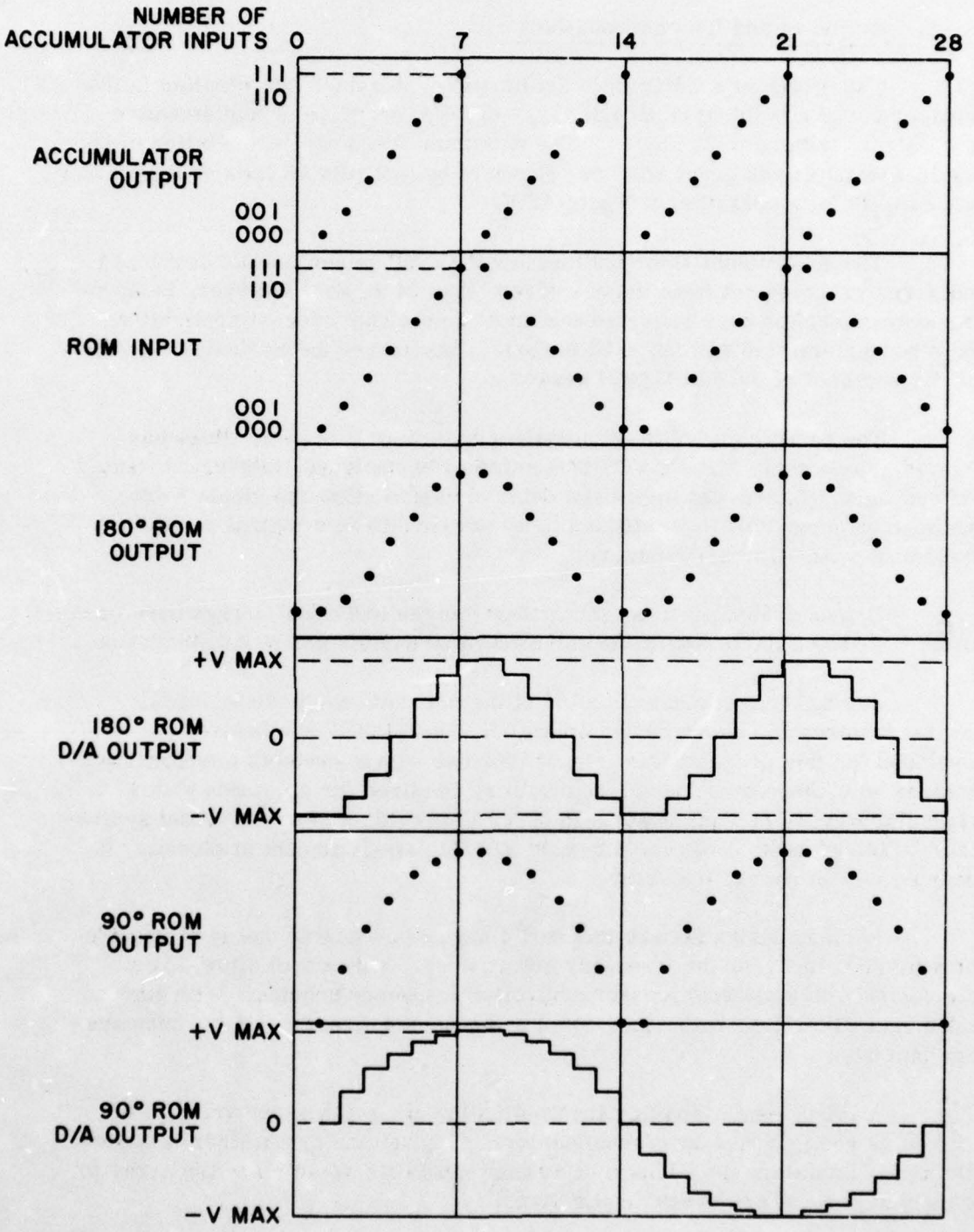


Figure 48. Arithmetic synthesizer waveforms.

6. Summary and Recommendations

The design of a CMOS/SOS arithmetic synthesizer has resulted in the development of a building block LSI array (TCS047) capable of implementing synthesizers with up to 32 stages. The maximum frequency of operation of the resultant synthesizer array has been shown to be typically 18 MHz at V_{DD} = 10 V with over 20 MHz operation at V_{DD} = 15 V.

The government specifications for the synthesizer module developed under this program requires the use of less than 24 stages, however, independent system studies have indicated that most known and forecast applications could be implemented with up to 32 stages. This served as the design objective for development of the CMOS/SOS array.

The partitioning of the synthesizer logic into four 8-bit slices has allowed a reasonably sized CMOS/SOS array to be designed, fabricated, tested and packaged. Internal switches and delay elements allow the single 8-bit synthesizer array type to be utilized in up to four different logical positions to implement a 32-stage synthesizer.

Demonstrated performance factors for the individual arrays have been within 10 percent of the estimates established by earlier computer simulation.

During the test and evaluation of the complete synthesizer module several features for future design emerged. The TCS047 synthesizer array developed for this program was intended for use with a sawtooth waveform synthesizer and, therefore, lacked the circuitry required for operation with a triangular waveform synthesizer. In order to provide a more universal synthesizer building block, it is recommended that this small amount of circuitry be incorporated as part of the array.

Another design feature that would have considerable use is to provide for a parallel input for the frequency select word. This would allow direct interfacing with a microprocessor controlled frequency scheme. With such an added capability, the synthesizer could be connected directly to a common system data bus.

A third design modification would allow the synthesizer array to be utilized as an eight bit adder/accumulator. Although the synthesizer is basically an accumulator, the addition of a reset capability would allow the array to be used in general arithmetic applications.

D. DIGITAL SYNTHESIZER MODULE

1. General Characteristics

a. Circuit Design Considerations

The design goals for the synthesizer system were established by the Government to be:

Center frequency (f_c):	200 kHz
Tuning range:	$\pm$12.5 kHz about f_c
Step resolution:	4 Hz minimum
Spectral purity:	See Figures 49 and 50
Settling time to 45° :	300 μs
Output:	Sine wave at +3 dBm (300 mV) minimum across 50 ohms.

As explained earlier in this report, a sawtooth waveform with constant period, slope and amplitude will always pass through the same voltage level as the AS staircase waveform relative to the AS clock. Thus, by considering any deviation from equality as an error voltage and using this error signal to control the period of a voltage controlled sawtooth generator, a phase-locked loop functioning as a synchronous sampler can be constructed whose output frequency is equal to the average frequency of the AS staircase and whose spurious level will be greatly reduced.

A block diagram of such a circuit is shown in Figure 51. The phase detector is a resistive adder which gives the algebraic sum between the AS staircase waveform and a sawtooth waveform of the opposite slope of the AS staircase. This error voltage, synchronously sampled by a delayed AS clock signal, is shown in Figure 52a. In Figure 52a the large voltage variations occur following a maximum to minimum voltage transition of either the staircase or sawtooth; sampling is not allowable between these two transitions. Although sampling can occur during each of the remaining small sawtooth variations, no improvement using multiple samples as opposed to a single sample was observed; hence, single sampling is used. The sample used is determined by the sample selector circuitry.

The sampled error voltage is held by the hold capacitor following the Sampler. This signal is amplified by the loop amplifier, filtered by the loop filter, and finally used to control the current magnitude of a constant current generator (CCG). The output of the CCG is integrated in a capacitor to derive the sawtooth ramp. The sawtooth is then formed when the level of the ramp equals the reference voltage causing activation of the dump circuit which

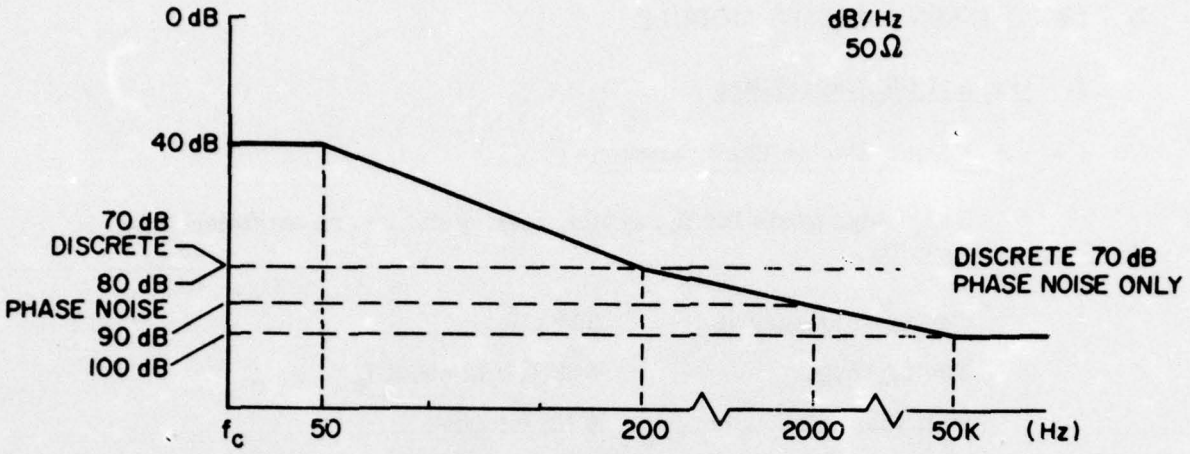


Figure 49. Close-in SSB spectral purity specification (phase noise and discrete in dB/Hz, 50 ohms).

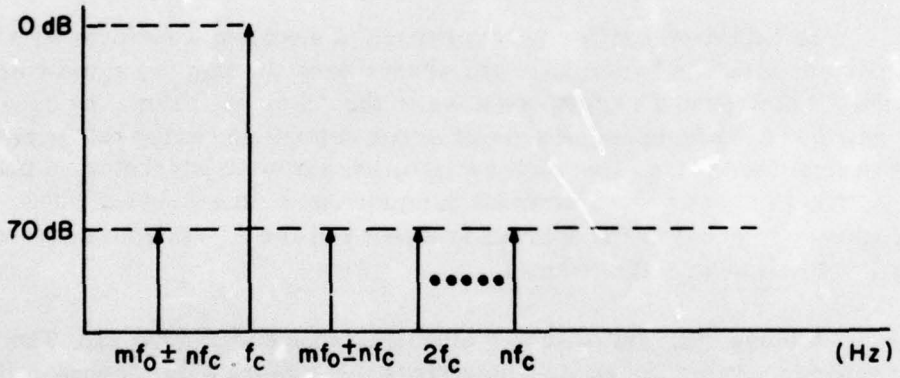


Figure 50. Wideband spectral purity (discrete) specification.

discharges the integrating capacitor over a period of approximately 60 ns. Following dumping, the dump circuit is reset, thereby allowing the CCG to begin charging the integrating capacitor again.

Buffer amplifiers are used to prevent loading and, hence, nonlinearities in the sawtooth waveform caused by other circuitry. The sawtooth is prefiltered in an RC network to prevent excessive ringing and overdrive of the output amplifier, filtered in a BPF to reduce harmonics and spurii far removed from the output frequency. Impedance transformation takes place in the emitter-follower (EF) on the output, and finally filtering to reduce harmonics generated in the EF is accomplished in the lowpass filter (LPF).

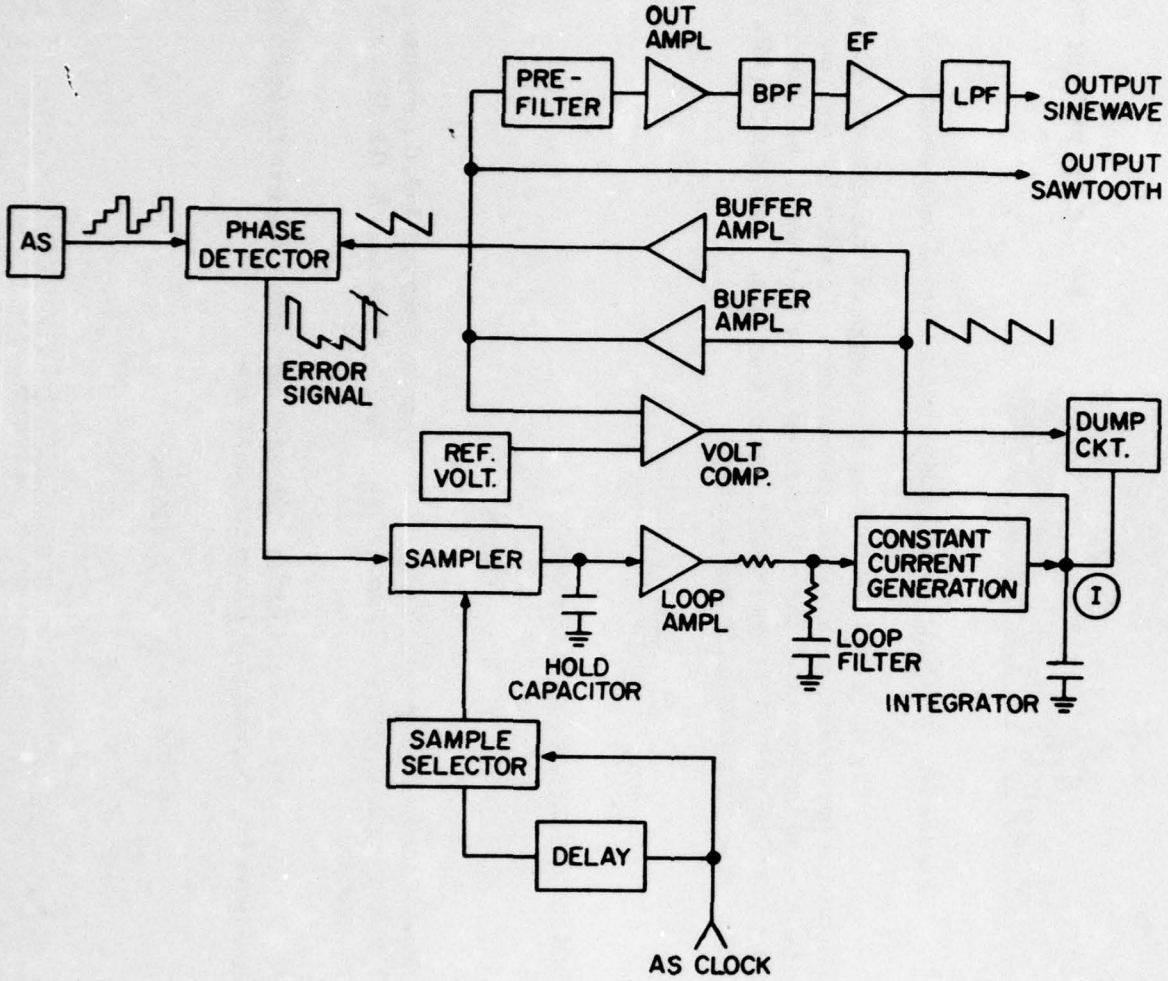
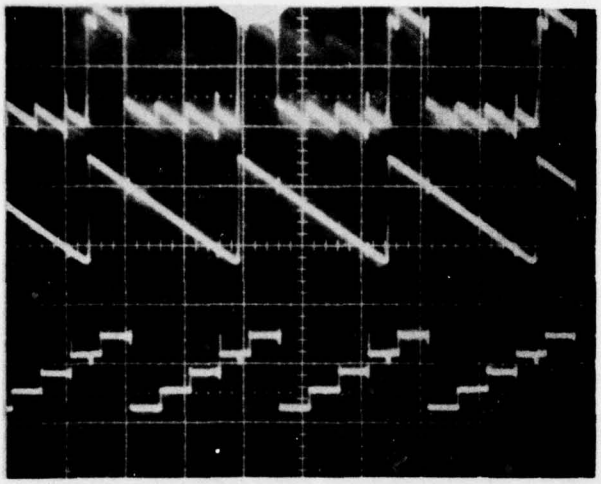


Figure 51. Block diagram of phase-locked loop (PLL).



(a) STAIRCASE U7-14

(b) SAWTOOTH Q6-4

(c) PHASE DIFFERENCE Q2-2

Figure 52. Arithmetic synthesizer/phase-locked loop waveforms.

The initial synthesizer module design efforts concentrated on establishing the phase-locked-loop (PLL) parameters. To allow for component tolerances and temperature, the pull-in range of the PLL should be approximately 50 percent more than the operating range of 25.0 kHz. Assigning 40 kHz to this value, then the equation for pull-in range,

$$\Delta\omega_p = \sqrt{2\omega_n(2\delta K - \omega_n)} \text{ rad/s},$$

and the equation for lock-in range,

$$\Delta\omega_L = 2\delta\omega_n \text{ rad/s},$$

provide the basis for calculating the loop parameters for δ=1.0 (critical damping). Substituting $\Delta\omega_p = 2\pi$ (40E3) and $\Delta\omega_L = 2\pi$ (25E3) gives $\omega_n = 2\pi$ (12.5E3) and K = 240332.

For a second-order high-gain loop with a passive filter as shown in Figure 53, the remaining loop constants are

$$T_1 = \frac{K}{\omega_n^2} = 3.896\text{E-}5$$

$$T_2 = \frac{2\delta}{\omega_n} - \frac{1}{K} = 2.13\text{E-}5$$

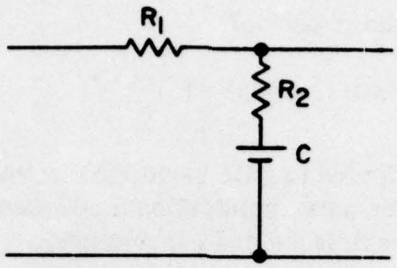


Figure 53. Loop filter.

Then

$R1 = 3757$ ohms

$R2 = 4532$ ohms

for $C = 4700$ pF.

$BW_{3dB} = 31$ kHz

$B_L = 51.1$ kHz

Where T_1, T_2, R_1, R_2 and C are as defined in Figure 53, BW_{3dB} is the closed loop bandwidth and B_L is the equivalent loop noise bandwidth.

The measured nominal sensitivity (K_v) of the sawtooth VCO was 210,000 radians per volt and the phase detector ($K\phi$) was 0.25 V/radian for an output of 1.6 V peak over 2π radians.

Each buffer amplifier has gain of approximately 0.8, thus requiring the loop amplifier to have a gain of $K_a = K/K_\phi K_v (0.8)^2 = 240332/0.25 (210E3) (0.8)^2 = 7.15$ V/V.

Laboratory tests of the AS/PLL using the above values proved to be slightly marginal for a ±20 kHz pull-in range. Through laboratory tests, the loop parameters required modification to obtain a ±20 kHz pull-in range with some design margin. Final values obtained were:

$K_\phi = 0.25$ V/radian

$K_a = 14.7$ V/V

K_v = 210,000 radians per volt

R_1 = 6kΩ; R_2 = 3kΩ; C = 4700 pF

Deviations were attributed to gain variations in the sawtooth VCO from band edge to band edge, buffer gain, unintentional attenuation, and loop bandwidth reduction due to stray resistance and capacitance.

For the above parameters, the final loop constants are:

$$K = 0.25\,(14.7)\,(210E3)\,(0.8)^2 = 493920$$

$$T_1 = 4.23E\text{-}5$$

$$T_2 = 1.41E\text{-}5$$

$$\omega_n = \sqrt{\frac{K}{T_1}} = 2\pi(29.798)K \text{ r/s} \quad \text{(the loop natural frequency)}$$

$$\delta = \frac{1}{2}\sqrt{\frac{K}{T_1}}\,(T_2 + \frac{1}{K}) = 1.5$$

$$\omega_L = 2\,(1.5\ \omega_n) = 2\pi\,(89.4)K \text{ radians/s}$$

$$\omega_p = \sqrt{2\omega_n\,(28K - \omega_n)} = 2\pi\,(110.81)K \text{ radians/s.}$$

Bode plots of the laboratory derived and theoretical cases are shown in Figure 54.

The phase error for a step frequency change (neglecting steady-state error) is:

$$\theta_e(t) = \frac{\Delta\omega}{\omega_n}\,(\omega_n t)\,e^{-\omega_n t}.$$

For $t = 300\ \mu s$, $\Delta f = \pm 25$ kHz and $\omega_n = 78539$ radians per second,

$$\theta_e(300\ \mu s) = 2(23.56)e^{-23.56}$$

$$= 2.76 \times 10^{-9} \text{ radian}$$

$$= 1.6 \times 10^{-7} \text{ degrees.}$$

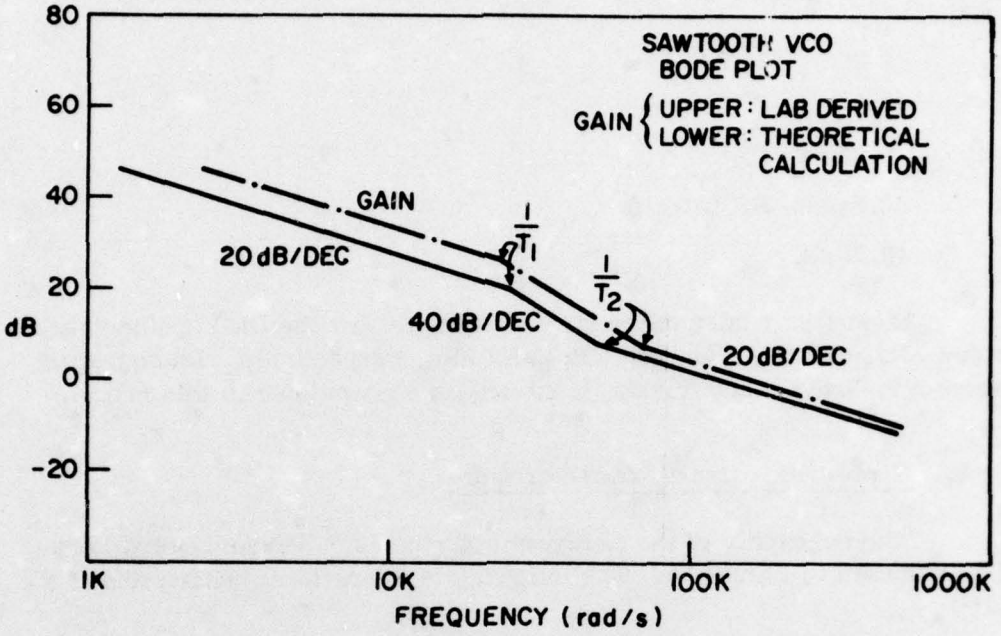


Figure 54. Bode plots for sawtooth VCO.

Conversely, for

$$\theta_e = 45°$$

$$t \simeq \frac{1}{\omega_n} = 12.7\ \mu s$$ for the sawtooth phase-locked loop to lock to within ±45° phase error for a frequency change of ±25 kHz.

The output bandpass filter has a nominal phase delay of 31 μs, plus 1.5 μs for the RC prefilter and output lowpass filter. Also for a change in the input frequency word, a delay of 8 μs (due to the storage registers after each accumulator) is incurred when operating at a clock frequency of 1 MHz before the new frequency appears at the DAC input.

The total accumulated delay is:

8 μs	TCS 047
0 μs	DAC
12.7 μs	PLL
32.5 μs	filters
53.2 μs	calculated lock time to within ±45° of steady-state after a maximum frequency change (±25 kHz).

For a frequency change of 1 kHz, the calculated lock time is:

8 μs	TCS 047
0 μs	DAC
0.25 μs	PLL
32.5 μs	BP filter
40.75 μs.	

Measured values of the above lock times for the final synthesizer module are 75 μs and 20 μs for $\pm$25 kHz and 1 kHz, respectively. Photographs, measurement technique, and further discussion are given later in this report.

b. Circuit Partitioning and Operation

The schematic of the Arithmetic Synthesizer/Phase-Locked Loop (AS/PLL) is shown in Figure 55. The following is a functional description of the schematic:

(1) In the upper left area, U2, U3 and U4 are the 8-bit TCS047 AS arrays. Circuits to the left of these arrays are input level translators from TTL to CMOS voltages. Circuitry to the right is the reverse translation of CMOS to TTL.

(2) U7 is the DAC which converts the binary word output of the TCS047 to the staircase signal used as the reference phase signal in the phase detector.

(3) The phase detector consists of Q3, a pulse amplifier, and Q2, the sampling switch, which, at each pulse from Q3, samples the algebraic sum of the reference staircase and the sawtooth derived at the junction of R15/C1 and R43/C13. This sample is stored on C8.

(4) The loop amplifier provides the additional loop gain necessary (over that of the VCO, phase detector, and source follower) to raise the level of the sampled error signal on C8 sufficiently to drive the sawtooth VCO constant-current generator.

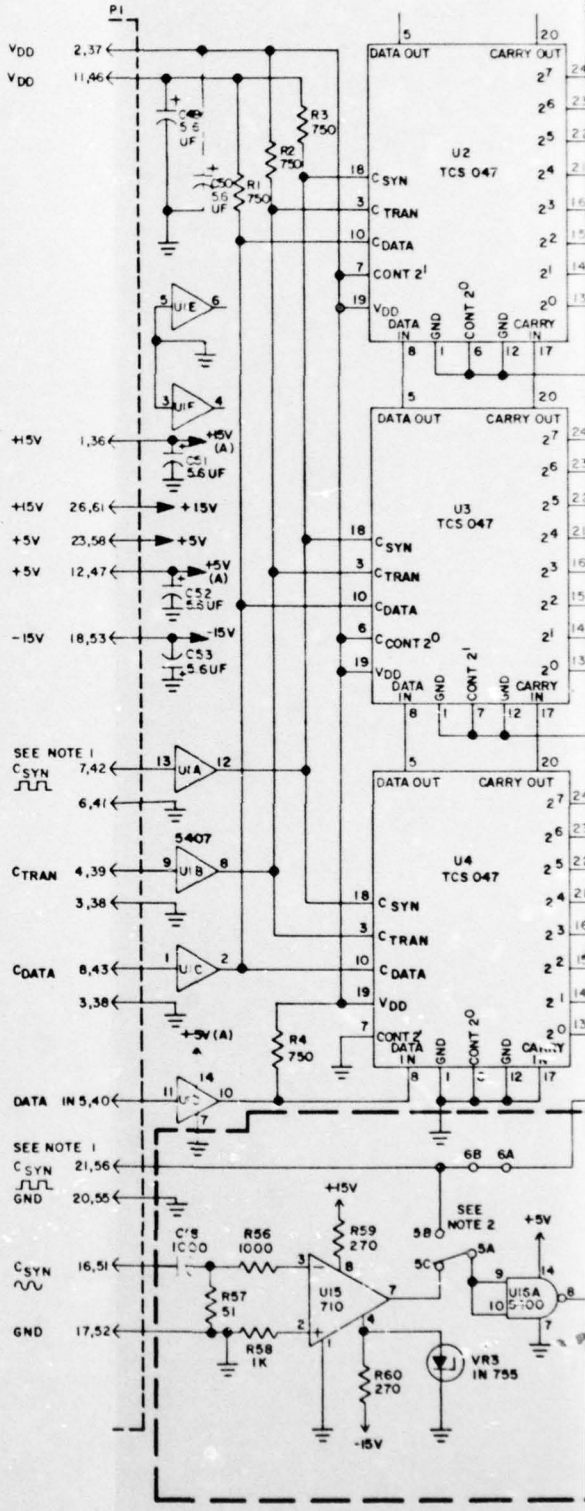
(5) The amplified signal above is integrated in the loop filter (R75, R76, C28), the output of which drives the constant-current generator, Q8. The output of Q8 is integrated in C29 to generate a voltage ramp. A sawtooth is generated across C29 by the dumping action of the sawtooth level reset detector.

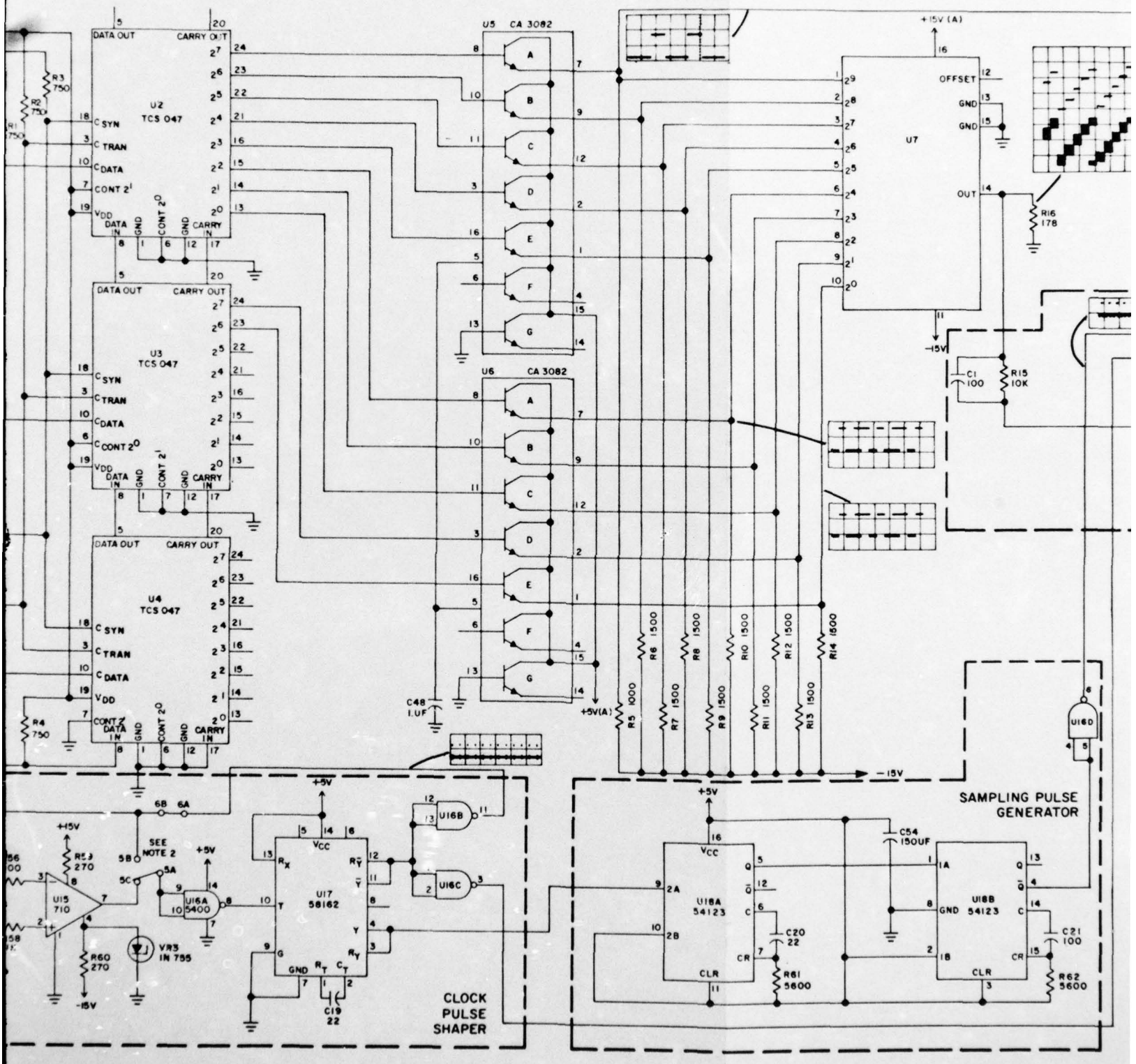
(6) When the voltage across C29 reaches a level set by R45 of the sawtooth reset level detector, U14 switches state, causing Q5 to conduct heavily, thus dumping C29 to generate the sawtooth VCO signal.

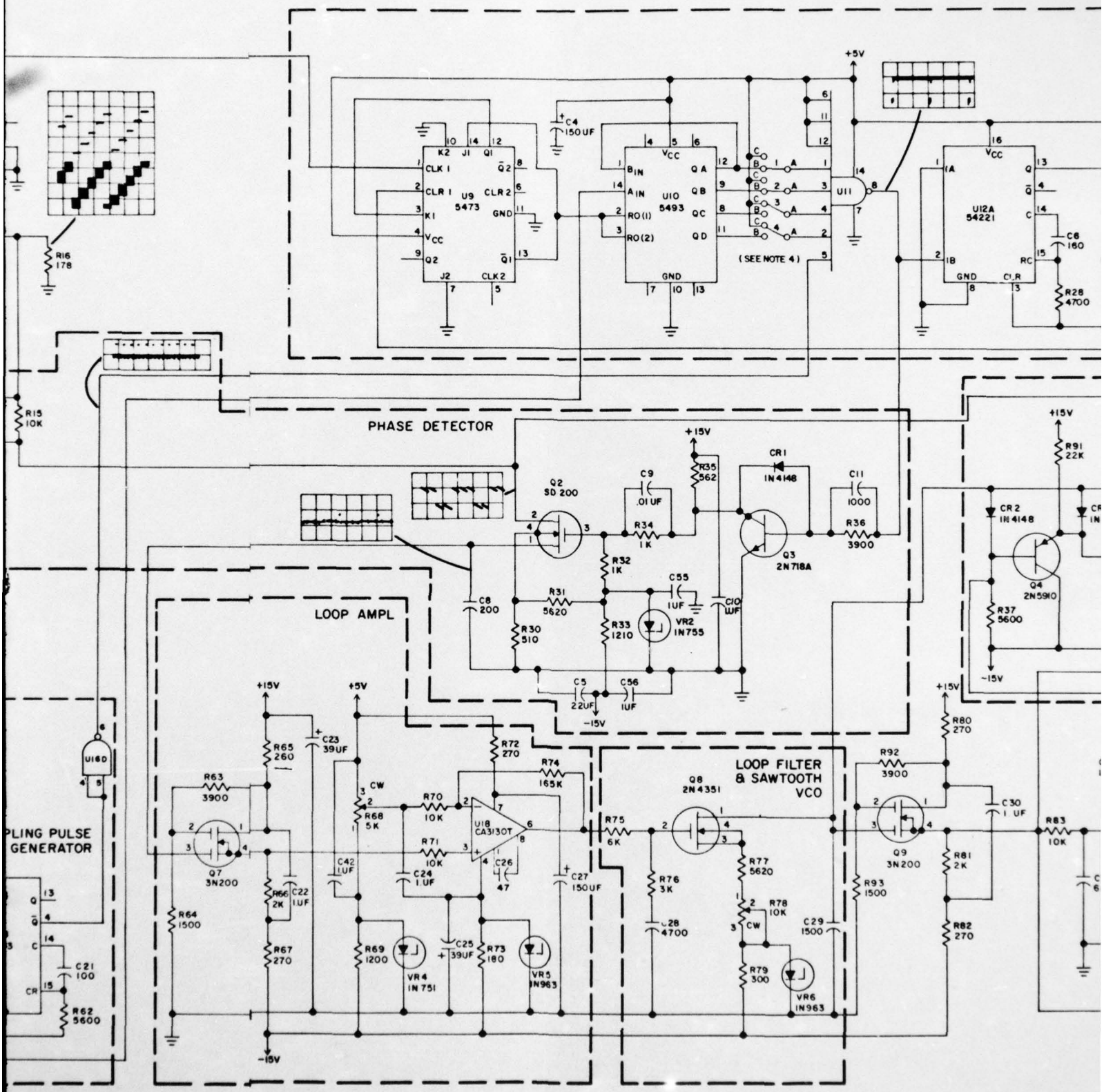
AS

NOTES

1. CONNECT PI-7 TO PI-21 EXTERNALLY ON MATING CONNECTOR.
2. FOR SINUSOIDAL C syn
   - A. CONNECT SINUSOIDAL C syn TO PI-16 THROUGH EXTERNAL MATING CONNECTOR.
   - B. ADD JUMPER 5 FROM C TO A AT OUTPUT OF U15, LEAVE OTHER JUMPER 5 POSITIONS OPEN.
   - C. ADD JUMPER 6 FROM B TO A AT OUTPUT OF U16B.
   - D. NO EXTERNAL CONNECTIONS OTHER THAN JUMPER IN NOTE 1 SHOULD BE MADE TO PI-7 OR PI-21.
3. FOR PULSE TYPE C syn
   - A. CONNECT PULSE C syn TO PI-7 OR PI-21 THROUGH EXTERNAL MATING CONNECTOR.
   - B. ADD JUMPER 5 FROM B TO A AT OUTPUT OF U15, LEAVE OTHER JUMPER 5 POSITIONS OPEN.
   - C. REMOVE ANY JUMPER 6 FROM B TO A AT OUTPUT OF U16B.
   - D. NO EXTERNAL CONNECTIONS SHOULD BE MADE TO PI-16 EXCEPT GROUND
4. JUMPERS 1 THROUGH 4 AT INPUT TO U11 CONNECTED FOR 200 KHZ NOMINAL OUTPUT FREQUENCY AND 1 MHZ C syn. CONSULT FINAL REPORT FOR DIFFERENT FREQUENCIES.
5. ALL C's IN PF UNLESS NOTED, CHECK PARTS LIST FOR C TYPE.
6. ALL L's IN uHY UNLESS NOTED.
7. CHECK PARTS LIST FOR RESISTOR WATTAGE AND TYPE.
8. CONNECT THE FOLLOWING VOLTAGE PINS TOGETHER ON EXTERNAL MATING CONNECTOR, PI-2 TO PI-11, PI-1 TO PI-26, PI-12 TO PI-23 AND PI-3, PI-6, PI-17, PI-20, PI-38, PI-41, PI-52 AND PI-55 TO POWER SUPPLY GROUNDS
9. RECOMMENDED GROUND CONNECTION FOR SIGNAL COAX SHIELD IS INDICATED BELOW EACH SIGNAL PIN ON P1.




AS
DAC
U2 TCS 047
U3 TCS 047
U4 TCS 047
U5 CA 3082
U6 CA 3082
U7
DATA OUT
CARRY OUT
C SYN
C TRAN
C DATA
CONT 2^1
CONT 2^0
VDD
DATA IN
GND
CARRY IN
+15V (A)
OFFSET
OUT
R1 750
R2 750
R3 750
R4 750
R5 1000
R6 1500
R7 1500
R8 1500
R9 1500
R10 1500
R11 1500
R12 1500
R13 1500
R14 1500
R15 10K
R16 178
C1 100
C48 1.UF
+5V(A)
-15V
+5V
+15V
SEE NOTE 2
U15 710
U16A 5400
U16B
U16C
U16D
U17 58162
VR3 IN 755
R59 270
R60 270
C19 22
CLOCK PULSE SHAPER
U18A 54123
U18B 54123
C20 22
C21 100
C54 150UF
R61 5600
R62 5600
SAMPLING PULSE GENERATOR


PHASE DETECTOR
LOOP AMPL
LOOP FILTER & SAWTOOTH VCO
+5V
+15V
-15V
U9 5473
U10 5493
U11
U12A 54221
(SEE NOTE 4)
Q2 SD 200
Q3 2N718A
Q4 2N5910
Q7 3N200
Q8 2N4351
Q9 3N200
U18 CA3130T
U16D
CR1 IN4148
CR2 IN4148
VR2 IN755
VR4 IN751
VR5 IN963
VR6 IN963
R16 178
R15 10K
R91 22K
R35 562
R34 1K
R32 1K
R31 5620
R30 510
R33 1210
R36 3900
R37 5600
R65 260
R63 3900
R72 270
R74 165K
R70 10K
R68 5K
R71 10K
R66 2K
R67 270
R64 1500
R69 1200
R73 180
R75 6K
R76 3K
R77 5620
R78 10K
R79 300
R80 270
R92 3900
R81 2K
R82 270
R93 1500
R83 10K
R62 5600
C4 150UF
C9 .01 UF
C11 1000
C8 200
C55 1UF
C10 1UF
C5 22UF
C56 1UF
C23 39UF
C22 1UF
C42 1UF
C24 1.UF
C26 47
C27 150UF
C25 39UF
C28 4700
C29 1500
C30 1 UF
C21 100
C6 160
R28 4700

AD-A040 156 RCA ADVANCED TECHNOLOGY LABS CAMDEN N J F/G 9/5
DIGITAL SYNTHESIZER AND CODE GENERATOR.(U)
JUN 76 H W KAISER, W F GEHWEILER, J I PRIDGEN F33615-74-C-1123
UNCLASSIFIED ATL-CR-76-03 AFAL-TR-76-123 NL

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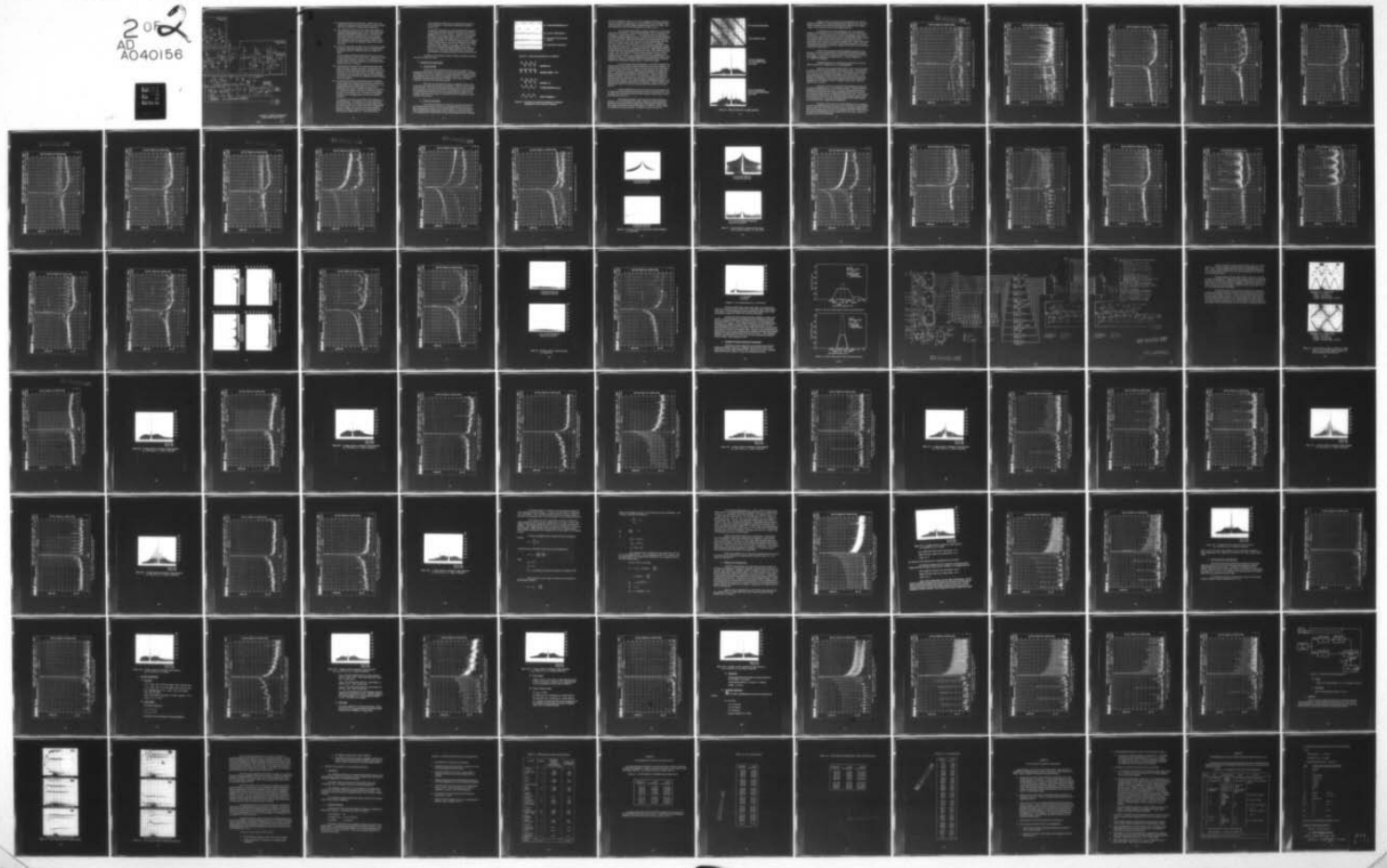
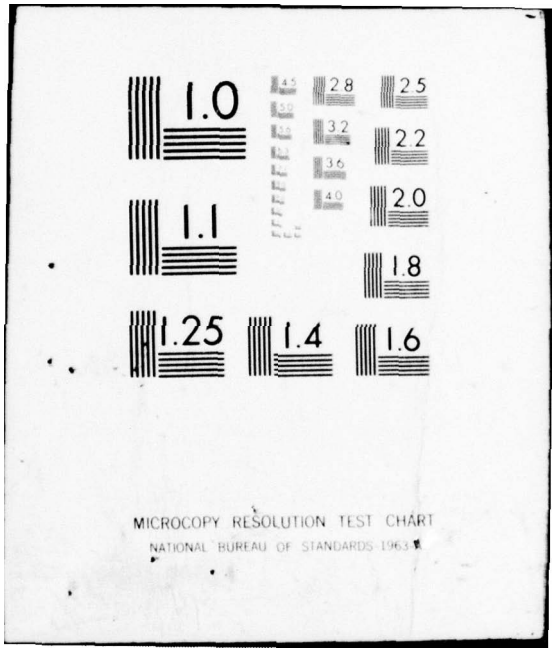



1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963

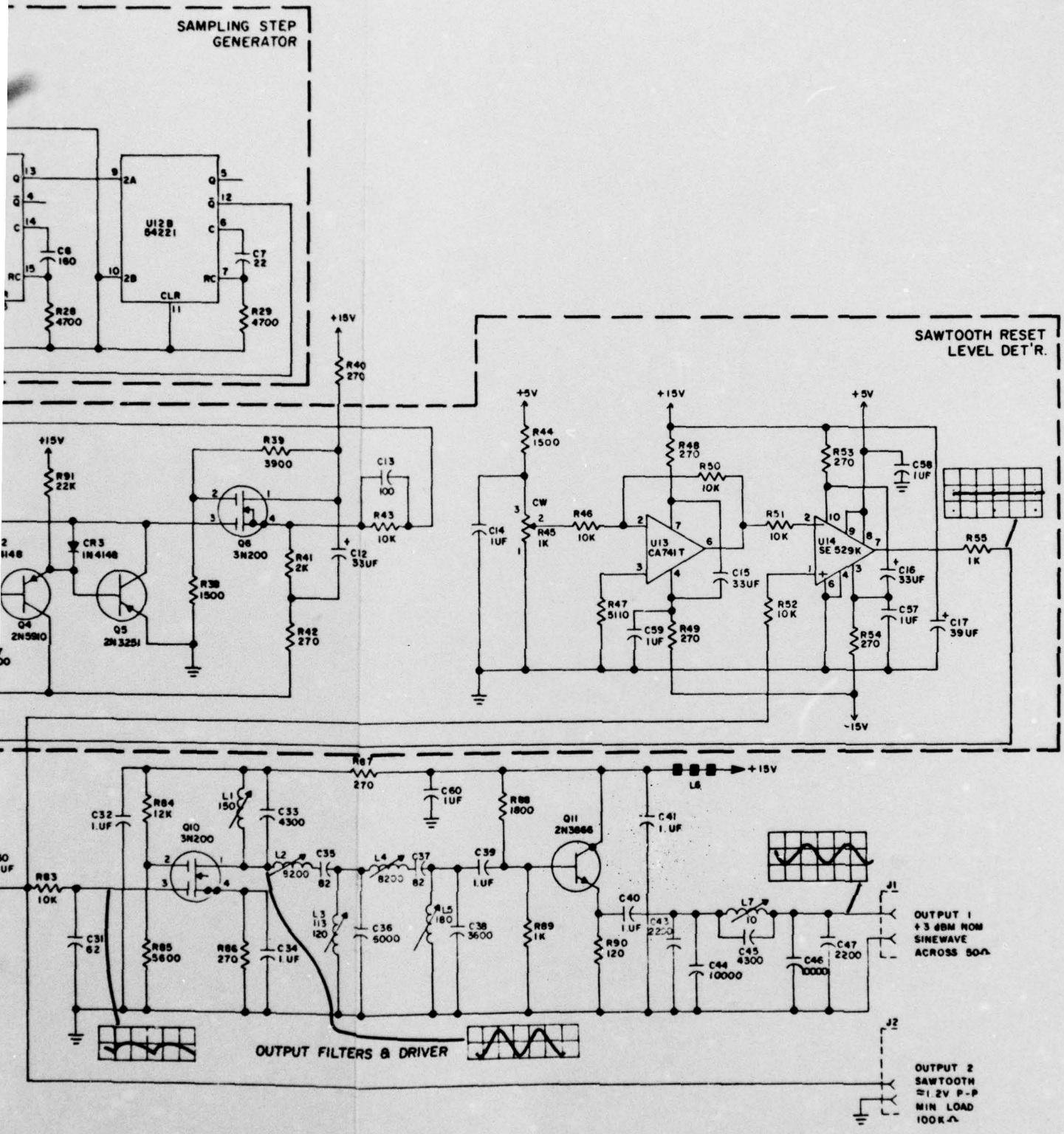


Figure 55. Arithmetic synthesizer/ phase-locked loop (AS/PLL).

(7) Miscellaneous circuitry includes Q6, a buffer between the sawtooth VCO signal and the phase detector, and Q9, a buffer between the sawtooth VCO signal and the output filter.

(8) The output filter consists of an RC section preceding Q10 to prevent ringing transients in Q10, a fifth-order unbalanced impedance Tchebycheff bandpass filter (L1 through L5 and C33 to C38) driving the output driver Q11 and a lowpass Cauer filter (C43-C47 and L7) for harmonic suppression. The synthesizer output is 3 dBm minimum across a 50-ohm ±5%, 100-pF load over the frequency range of 187.5 kHz to 212.5 kHz.

(9) In the lower left corner of Figure 55 is the clock pulse shaper. By proper positioning of jumpers 5 and 6, the input clock to the AS/PLL may be a 1-MHz sine wave or a 1-MHz TTL signal.

For an external sinusoidal synthesizer clock (C_{syn}) the connections of jumpers 5 and 6 are as shown. Pins 21 and 7 must be externally connected at all times. For pulse type C_{syn}, jumper 6 must be removed and jumper 5 connected from A to B rather than A to C as shown.

(10) Following the above circuit is the sampling pulse generator which generates a delayed clock pulse. The purpose of the delay is to inhibit sampling in the phase detector until the output of the DAC (U7) has settled down. This delay is approximately 300 ns and thus limits the maximum clock frequency to 3.5 MHz for the sawtooth wave synthesizer module designed under this program.

(11) The delayed clock pulse mentioned previously is combined with the output of the sampling step generator to generate the sampling pulse for the phase detector at the input to Q3. The sampling step generator determines how many clock pulses occur (by counter U10) after the staircase is reset to 0 V and before a sample is taken by the location of jumpers 1 through 4 (at the inputs to U8). The number of clock pulses has been set at 3 or approximately one-half the staircase amplitude.

The jumpers at U8 have been provided to allow adjustment of the sampling time. For example, if the clock frequency is increased to 3 MHz, then three times as many steps occur in the staircase relative to a 1-MHz clock (12 to 15 steps rather than 4 to 5 steps). For this case, the jumpers should be selected to recognize a count of seven (approximately one-half staircase voltage) from U10. This may be done by

removing jumper 3 from its A-C connection and placing it in the A-B position. U12 provides a delay before resetting counter U10.

To generate a frequency, f_o, the serial digital data representing the frequency control word N_f in binary format of 24 bits is applied to PI-(5, 40), "Data In." This data is then clocked, MSB first into the storage register of the AS (U2 through U4) by 24 pulses of data clock "C_{data}" (PI-(8, 43)), whose rate may be up to 20 MHz. When the LSB of the N_f has been clocked into the storage register, N_f is then transferred to the holding register by clock "C_{trans}" (PI-(4, 39)). This N_f word is then processed at each pulse of the synthesizer clock, C_{syn} (PI-(7, 42)) to produce the binary equivalent of the AS output frequency, f_o. Conversion of this binary word to the staircase waveform of average frequency f_o is done by the DAC (U7).

In addition to the waveforms shown in Figure 52, typical waveforms are shown in Figures 56 and 57.

2. Performance Characteristics

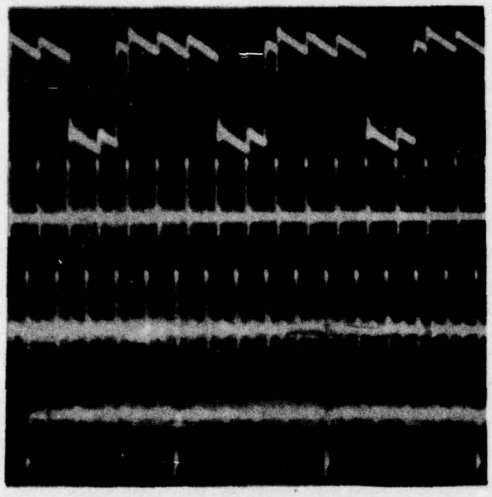
a. Test Philosophy

Since the TCS047 CMOS/SOS LSI array was not available at the beginning of this contract, a discrete TTL version of the synthesizer, developed previously by RCA in-house programs, was used to generate the staircase waveform reference signal to be used for development of the PLL. Although the TTL breadboard could be programmed up to 32 stages, only 24 bits were used in testing the circuitry for the synthesizer module.

Much data were accumulated using the breadboard and were used to determine PLL performance early in the contract. When the TCS047 arrays became available, they were incorporated into the synthesizer module circuitry and comparisons were made between the two technology types of synthesizers. No major spectrum differences were noted and all spectrum response curves included in this report were taken on a deliverable AS/PLL synthesizer module using the TCS047 arrays.

b. AS/PLL Test Results

Tests using the discrete AS with the PLL and later with the TCS-047 SOS chip version of the AS with the PLL indicated that the clock and the phase sampling pulse widths were not critical; however, the delay between the clock pulse and phase sampling pulse must be sufficient to ensure that phase-error sampling does not occur before the DAC has completely settled. Although



(a) PHASE DIFFERENCE Q2-2

(b) CLOCK PULSE Q16B-11

(c) DELAYED CLOCK PULSE Q16D-6

(d) SAMPLING PULSE Q11-8

Figure 56. Arithmetic synthesizer/PLL waveforms

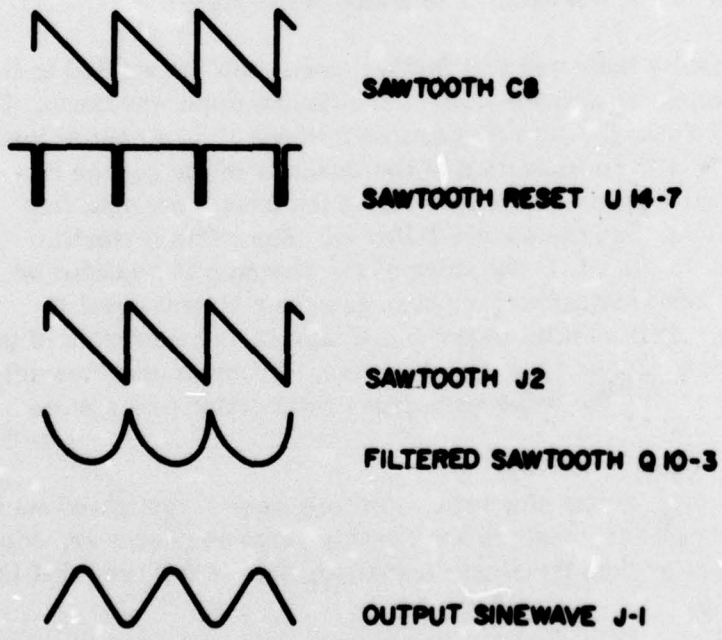


Figure 57. Miscellaneous arithmetic synthesizer waveforms. (Designations refer to Figure 55 callouts.)

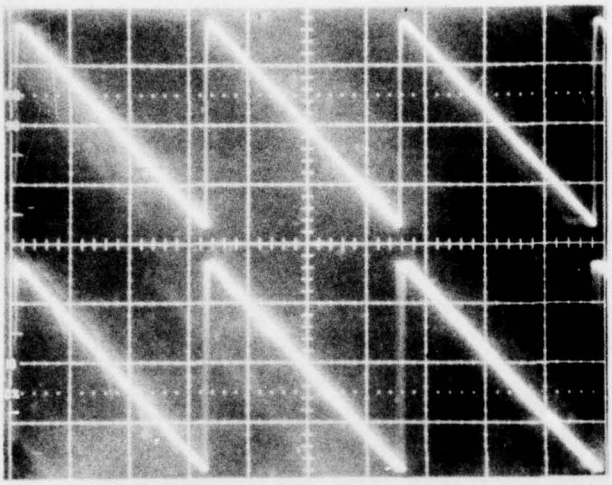
the DAC is specified to settle in 10 to 20 ns, sampling with delays of less than 100 to 200 ns after the clock pulse (or a step transition on the staircase) introduced new spurii or enhanced spurii already present in the PLL output. This delay effectively limits the clock frequency to 3.5 MHz or less.

The most pronounced effect on spurious signals is the reset amplitude level of the sawtooth. For a 24-bit accumulator, an all 1's condition corresponds to a decimal number $2^{24}-1$. The output of the DAC for this input is the maximum output voltage of the DAC. The reset level of the sawtooth should be the DAC reference voltage and corresponds to the voltage produced by the decimal number 2^{24}. Since the reset time of the sawtooth is finite, this ideal case is not reached and the reset voltage is less than the 2^{24} voltage by $(T_r/T_s)(V)$ where T_r is the reset time, T_s is the sawtooth period and V is the DAC reference voltage level. This reset level voltage is generated by potentiometer R45 and IC U13 in the schematic in Figure 55. Rapid setting of R45 can be obtained by observing the phase difference waveform (see Figure 56a) at pin 2 of Q2. R45 is then adjusted to force the small sawtooth peaks to the same voltage level on the scope, i.e., with no horizontal tilt to a straight line connecting the peaks. More accurate adjustments can be obtained by observing the spectrum of a signal on a spectrum analyzer and adjusting R45 for a minimum of phase noise and spurious signals within 1 to 2 kHz of the signal.

The test results indicated that further work could be applied to the linearity of the source followers used as buffers for the sawtooth waveform. If a pure sinusoid is injected into the gate of a source follower, the output second harmonic is down 55 to 70 dB, an indication of the linearity of the source follower. This distortion will appear as a slight curvature from a straight line when the sawtooth is injected into the source follower. Since this distortion appears as a phase error to the PLL, the slope of the sawtooth is adjusted by the loop to force the sawtooth voltage at the phase sampling instant equal to that of a linear sawtooth. This results in phase and amplitude modulation of the sawtooth by the undesired components of the staircase. Problem spurious signals are down only 55 to 70 dB, the same as harmonic distortion of a source follower.

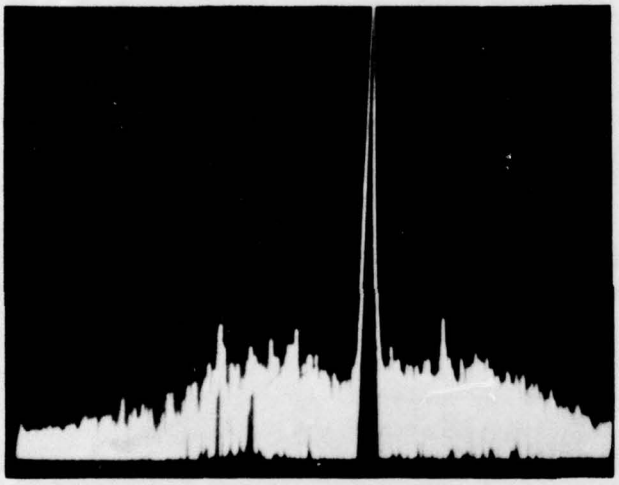
Various configurations of source followers were investigated such as single and cascade discrete transistors and op-amp versions; however, none was found with less distortion than the single transistor source follower that is currently used in the PLL.

The distortion problem is the reason the staircase itself is not isolated. Use of a source follower isolator, although no visually detectable distortion occurred, produced an enhancement of the spurious signals on the PLL output. Distortion of the sawtooth signal by the addition of shunt loading also enhanced the spurious signals. This effect is shown in Figure 58.

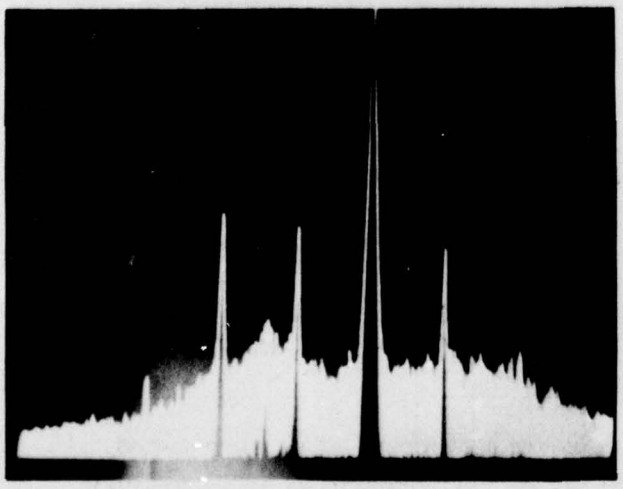


NO LOAD ON SAWTOOTH

330 K Ω SHUNT LOAD



OUTPUT SINEWAVE
NO LOAD SPECTRUM
212.5 KHz



OUTPUT SINEWAVE
330 K Ω LOAD SPECTRUM
212.5 KHz

Figure 58. Effects of distortion on output spectrum.

Spectrum plots of the final AS/PLL configurations are shown in Figures 59 through 84. In these photographs of the spectrum plots, the curve labeled "sawtooth" is the spectrum of the staircase while the curve labeled "output" is the spectrum of the sinusoid output of the PLL.

In all figures where 100/1000 appears in the "scan width/div" heading, the horizontal scale is 100 Hz/div to the left of f_o and 1000 Hz/div to the right of f_o. The left vertical scale is used to read spurious signal levels and the right vertical scale for phase noise in a 1-Hz bandwidth across 50 ohms. Also, spurious signal levels on the 1000 Hz/div horizontal plot must be increased by 6 dB to account for the plotter response time. Spikes immediately to the right of the analyzer f_o response (in most cases marked by an "X") are switching transients occurring when the analyzer sweep width was changed from 100 Hz/div to 1000 Hz/div.

Because of the amplitude and many spectral components of the staircase, some of the spectral lines on the 100 Hz/div portion are caused by the analyzer. These can be detected by their mirror image shape of the analyzer bandpass response at f_o (Figure 62 at f_o = 150 Hz, Figure 63 at f_o = 690 Hz, for example).

Wideband spectrums are also shown for frequencies where the spurious signals are of sufficient level to be photographed.

Figure 84 is the spectrum of the AS/PLL over a range of 200 kHz to 1 MHz to show the harmonic content of the output sinusoid. On Figures 66 and 71 the PLL has a discrete spurious at f_o + 8.5 kHz which does not appear on the spectrum of the staircase when plotted on the Adret analyzer. It is believed the explanation is that the spectrum of the staircase was a high PM deviation, low frequency, signal which overloads both the Adret and Hewlett-Packard (HP) (HP spectrum is shown in Figure 70) and, hence, masks the spurious at f_o + 8.5 kHz.

In general, the PLL provides 40 to 50 dB additional rejection of the undesired signals present in the staircase waveform. Deviation from this attenuation does occur and can be seen in several of the spectral responses. On the basis of data taken, the design goal spectral purity versus the worst case measured spectral purity is depicted in Figures 85 and 86. In most cases, the worst case limitations are caused by only several spurious signals rising to the indicated level. The limits expressed by these curves reflect mainly the worst case for the nonsynchronous frequencies.

During the work on the PLL, several different DACs were tested. All DACs with settling times greater than 100 na were found to be unsatisfactory. Only one other DAC, the DATEL model HI12B was comparable (approximately 50 to 60 ns settling time) to the DAC used (Computer Labs MDP-1020); however, the DATEL introduced higher spurious signal levels in the range ±5 kHz and greater from the center frequency.

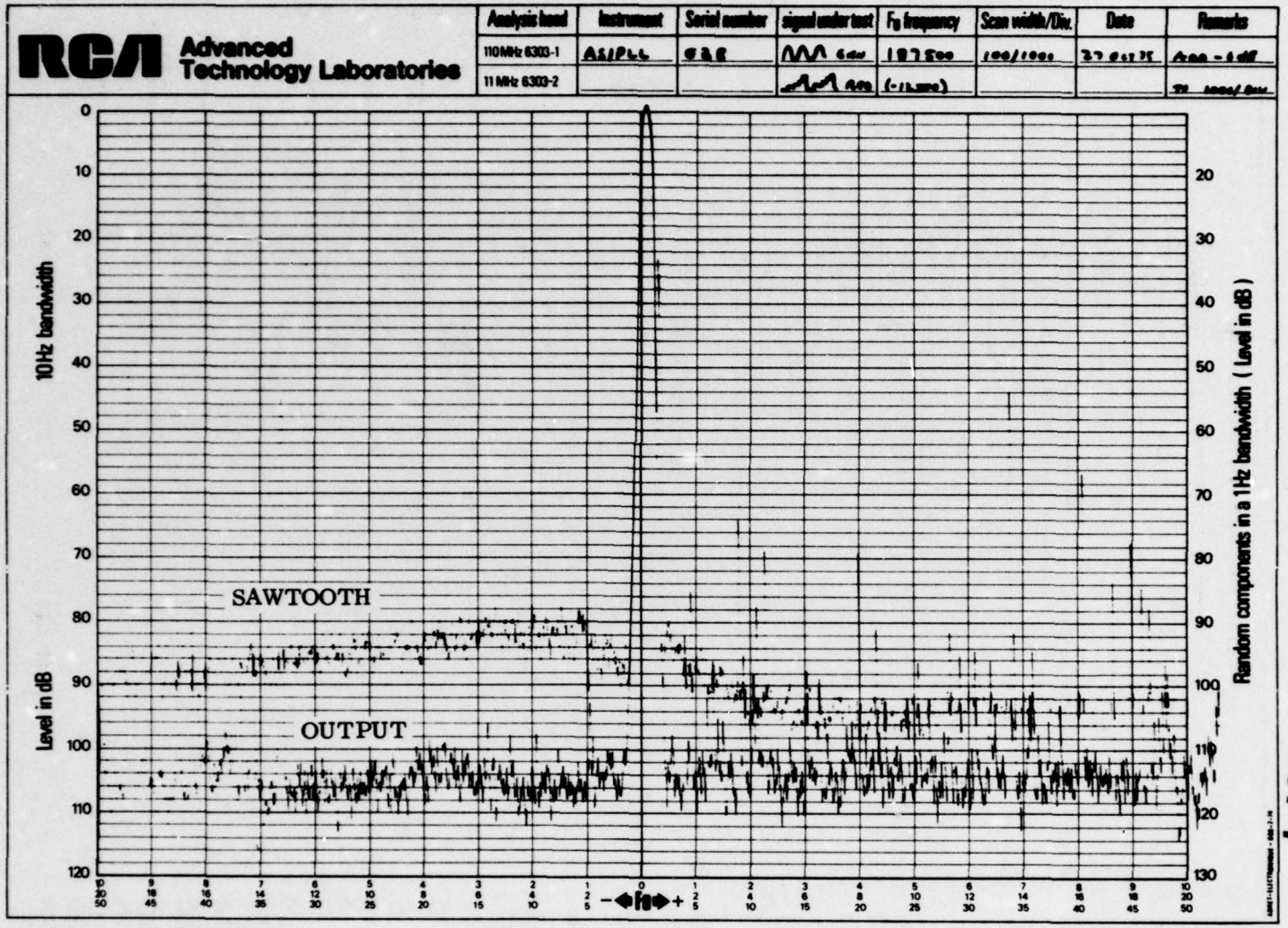


Figure 59. Sawtooth and output spectrum for f_o = 187, 500 Hz.

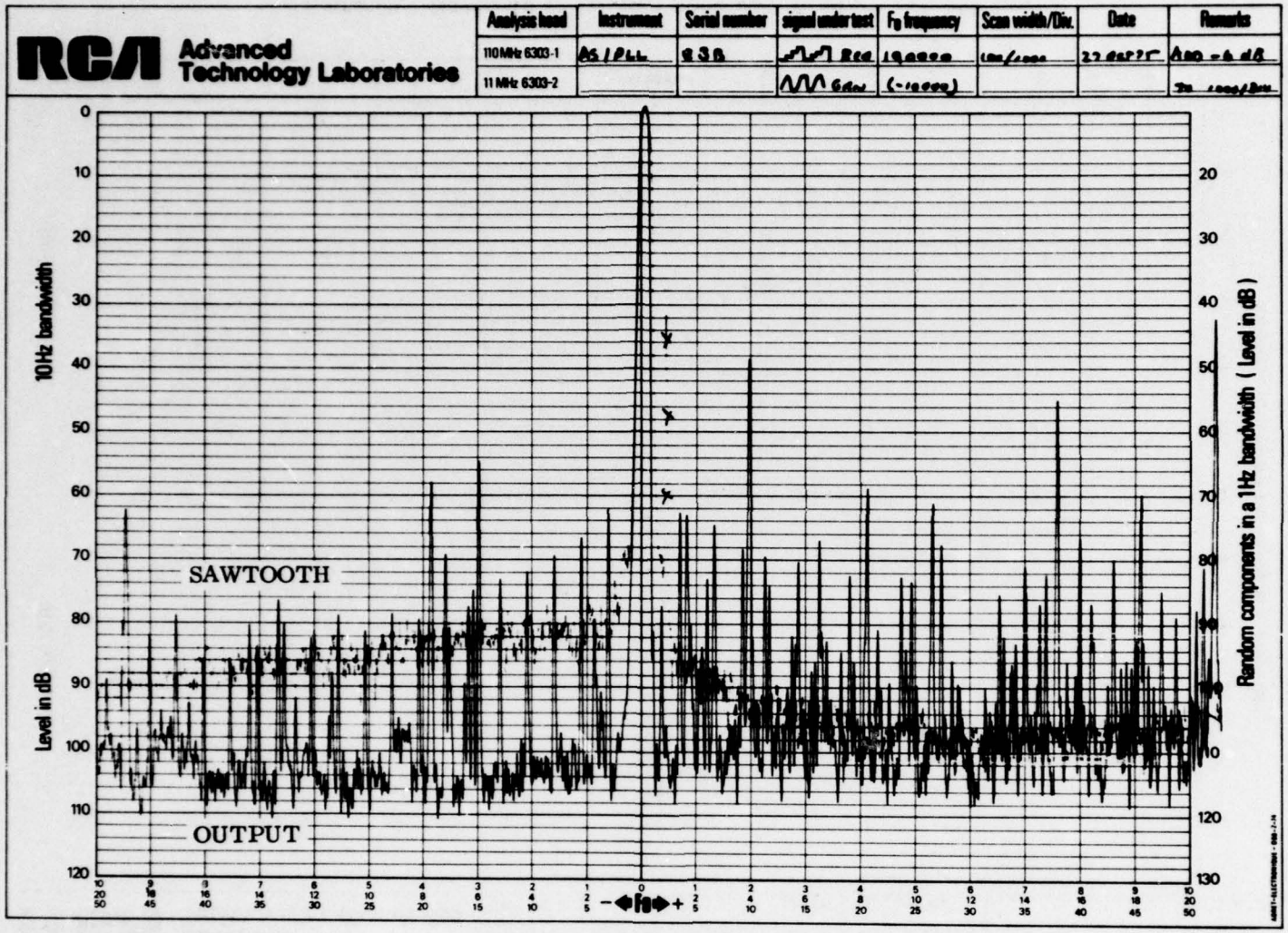


Figure 60. Sawtooth and output spectrum for f_o = 190,000 Hz.

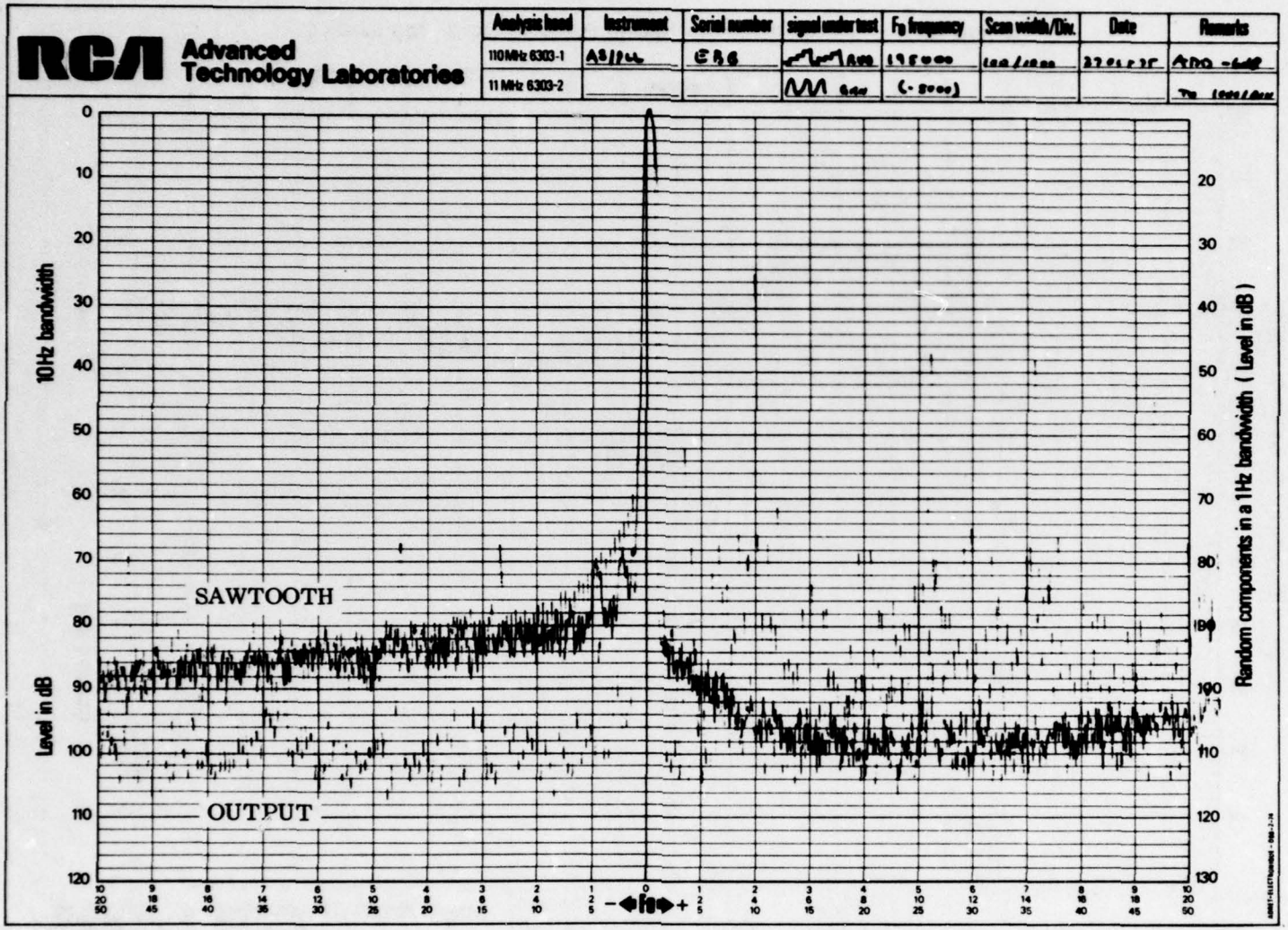


Figure 61. Sawtooth and output spectrum for f_o = 195,000 Hz.

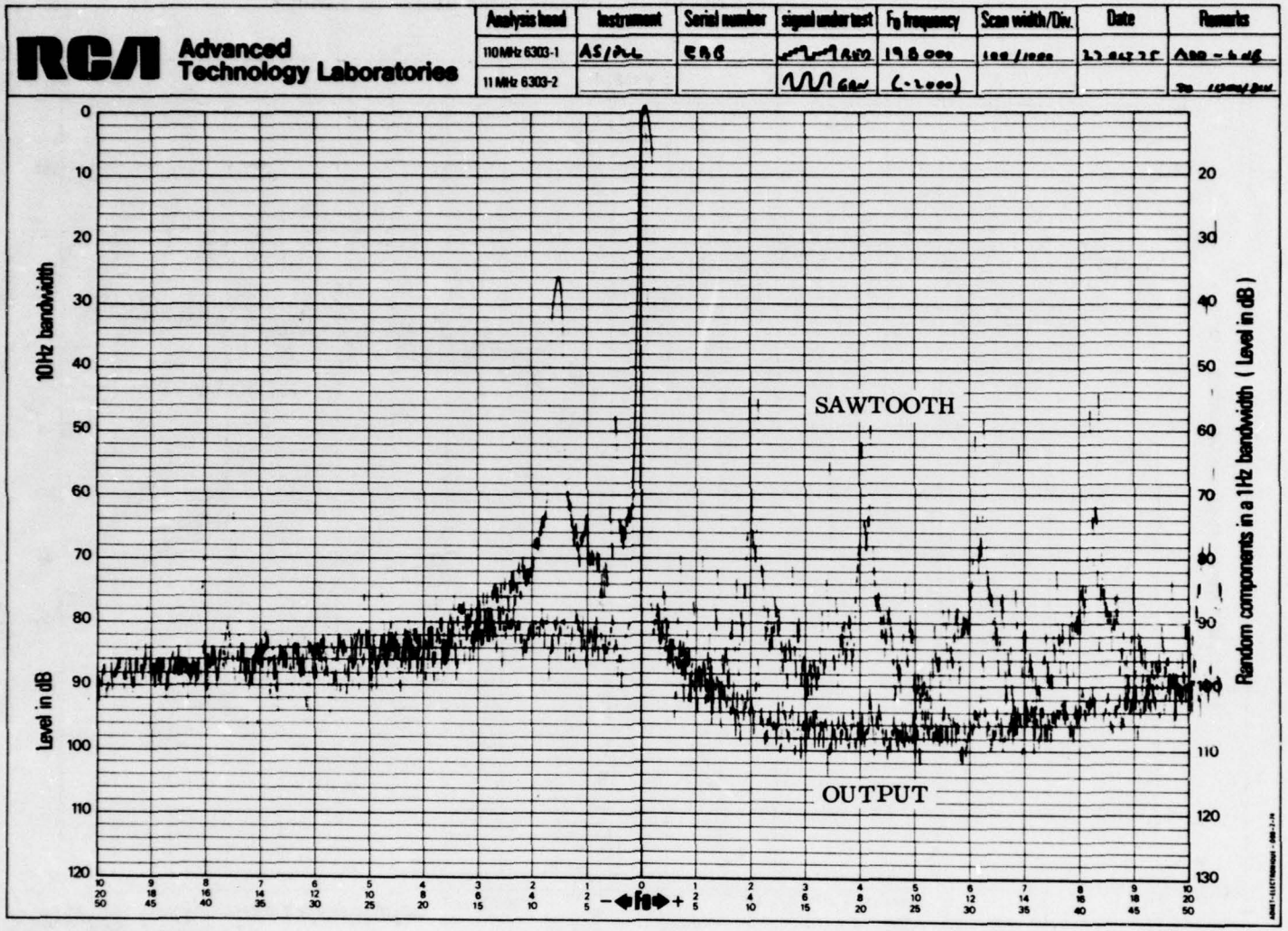


Figure 62. Sawtooth and output spectrum for f_o = 198,000 Hz.

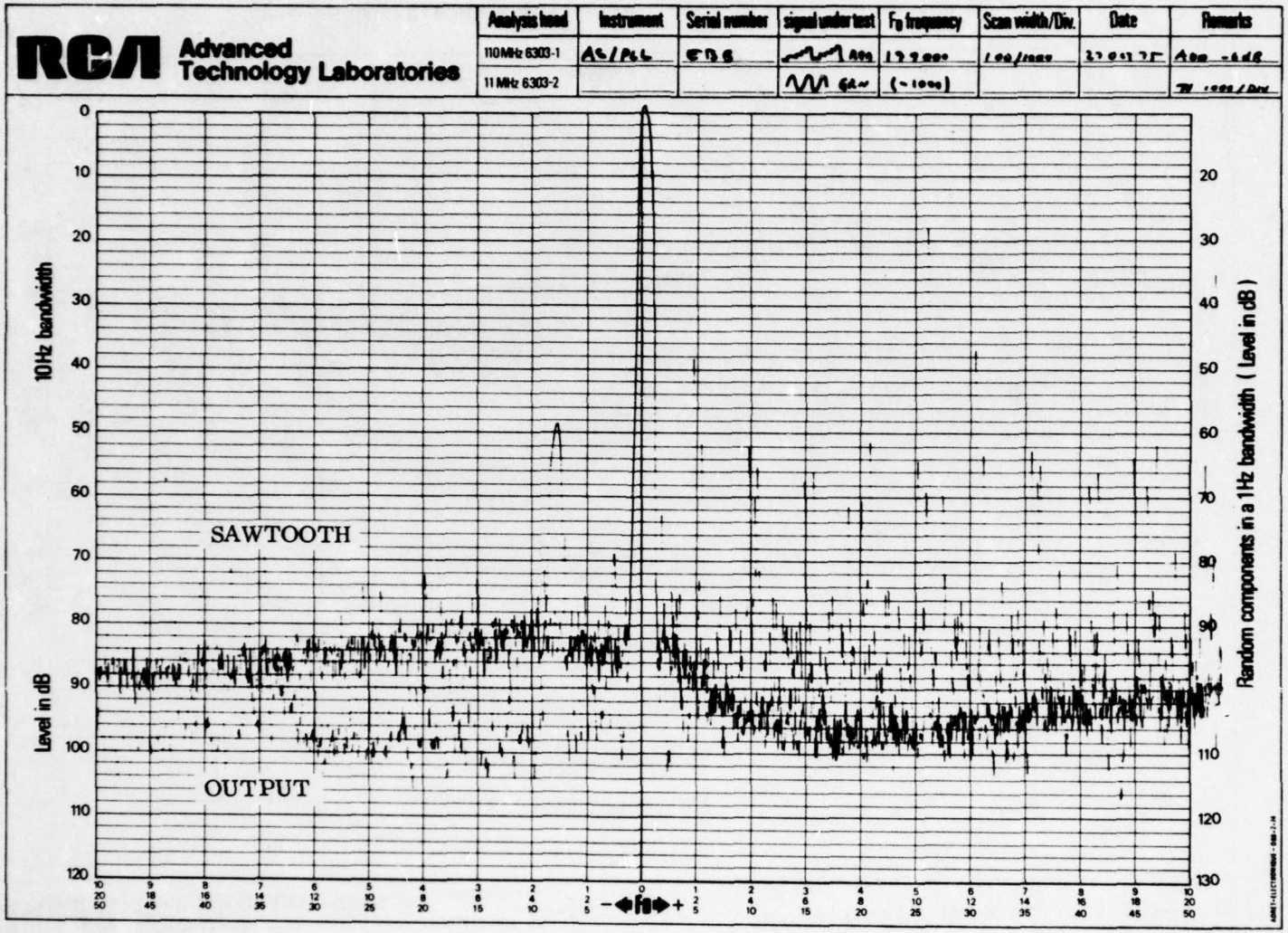


Figure 62. Sawtooth and output spectrum for f_o = 199,000 Hz.

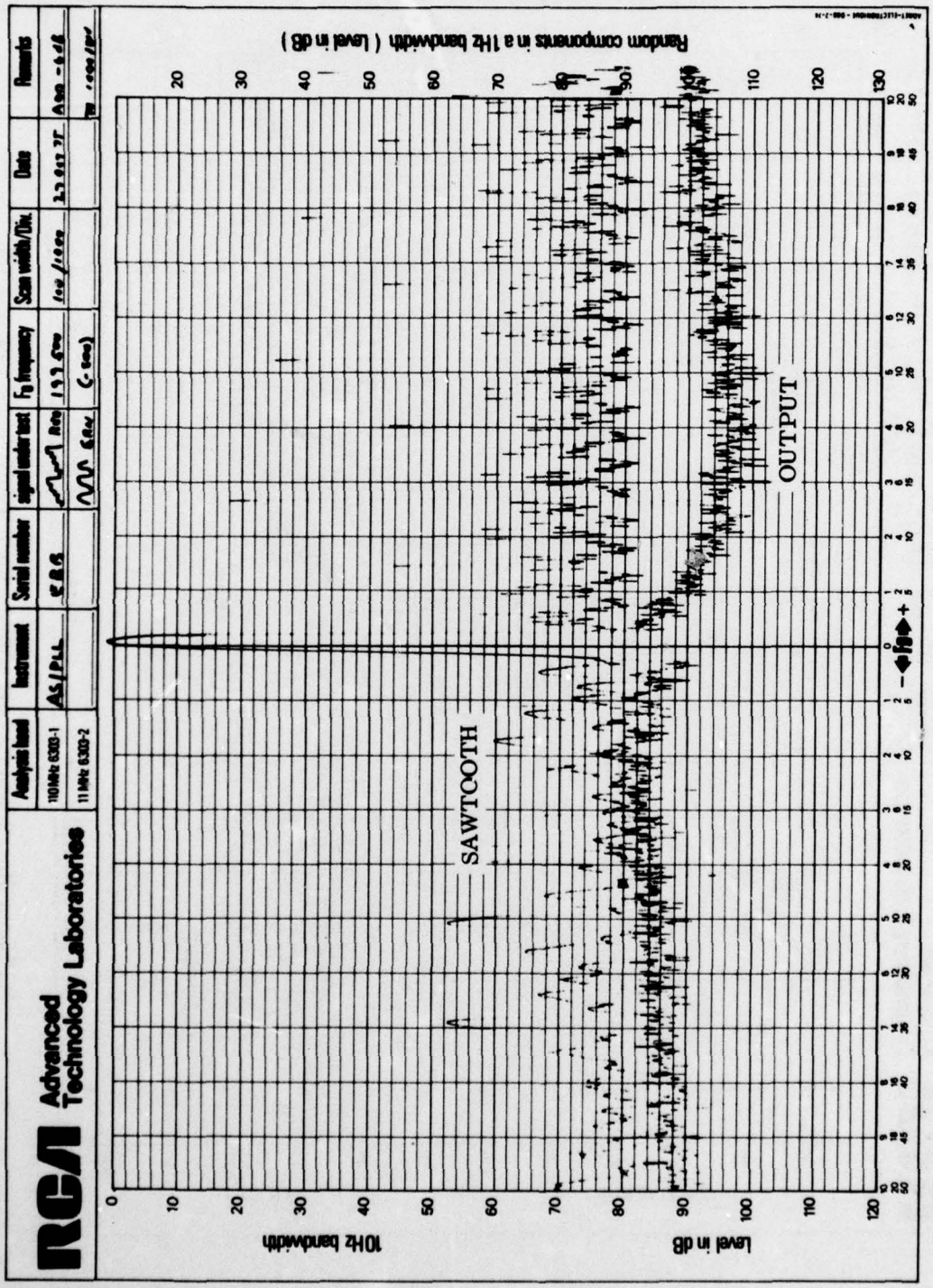


Figure 64. Sawtooth and output spectrum for f_o = 199, 500 Hz.

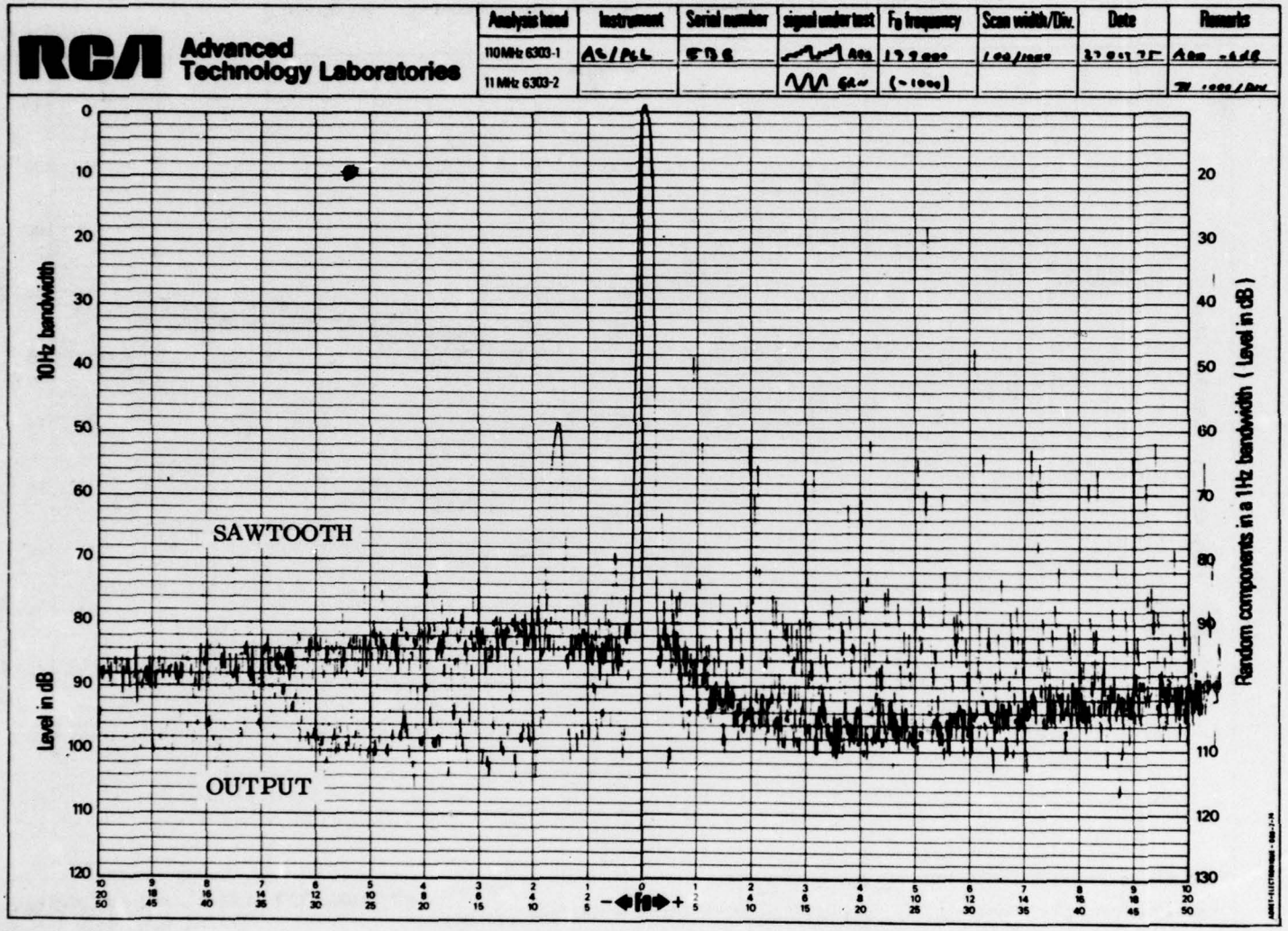


Figure 63. Sawtooth and output spectrum for f_o = 199,000 Hz.

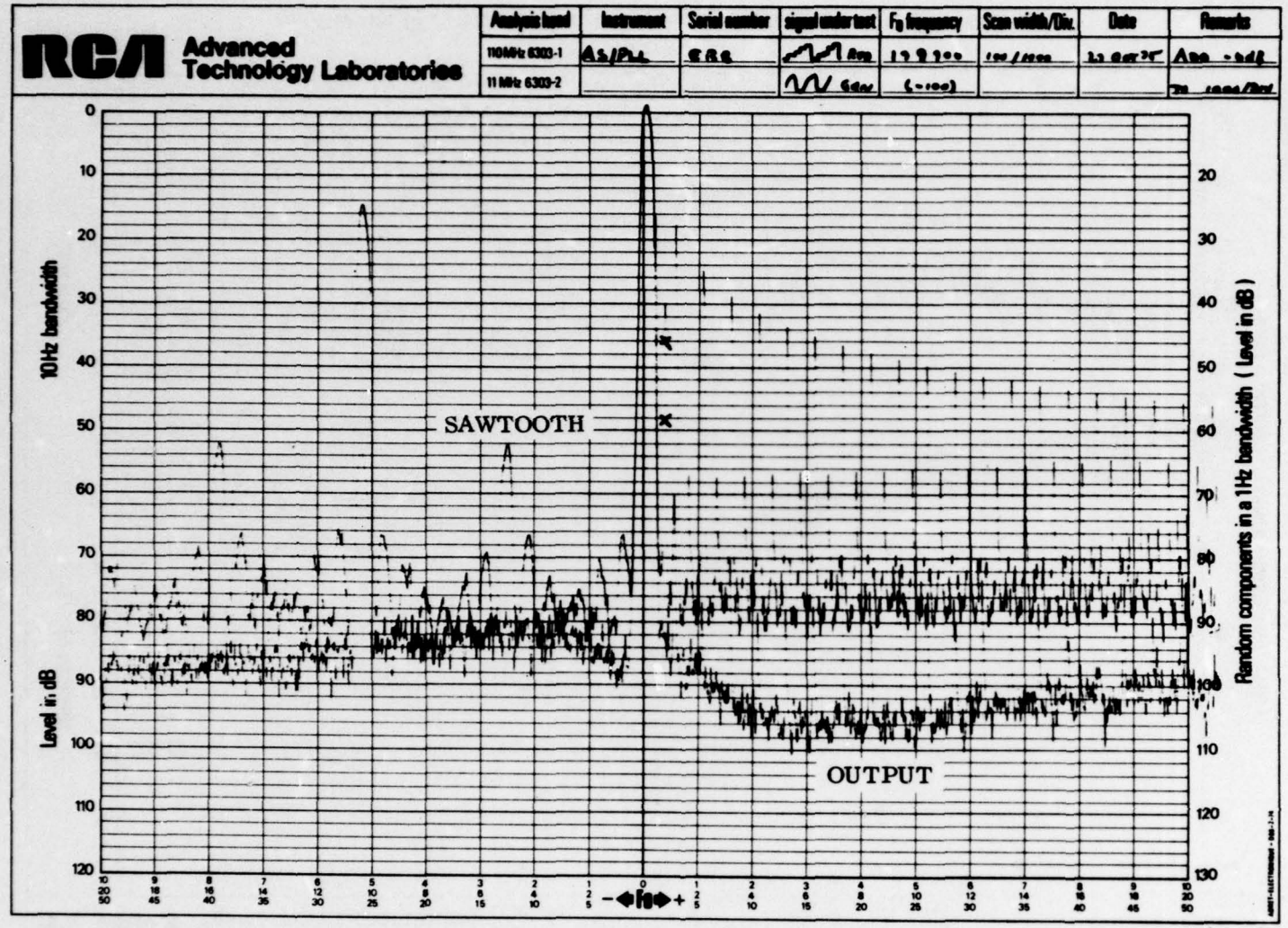


Figure 65. Sawtooth and output spectrum for f_0 = 199, 900 Hz.

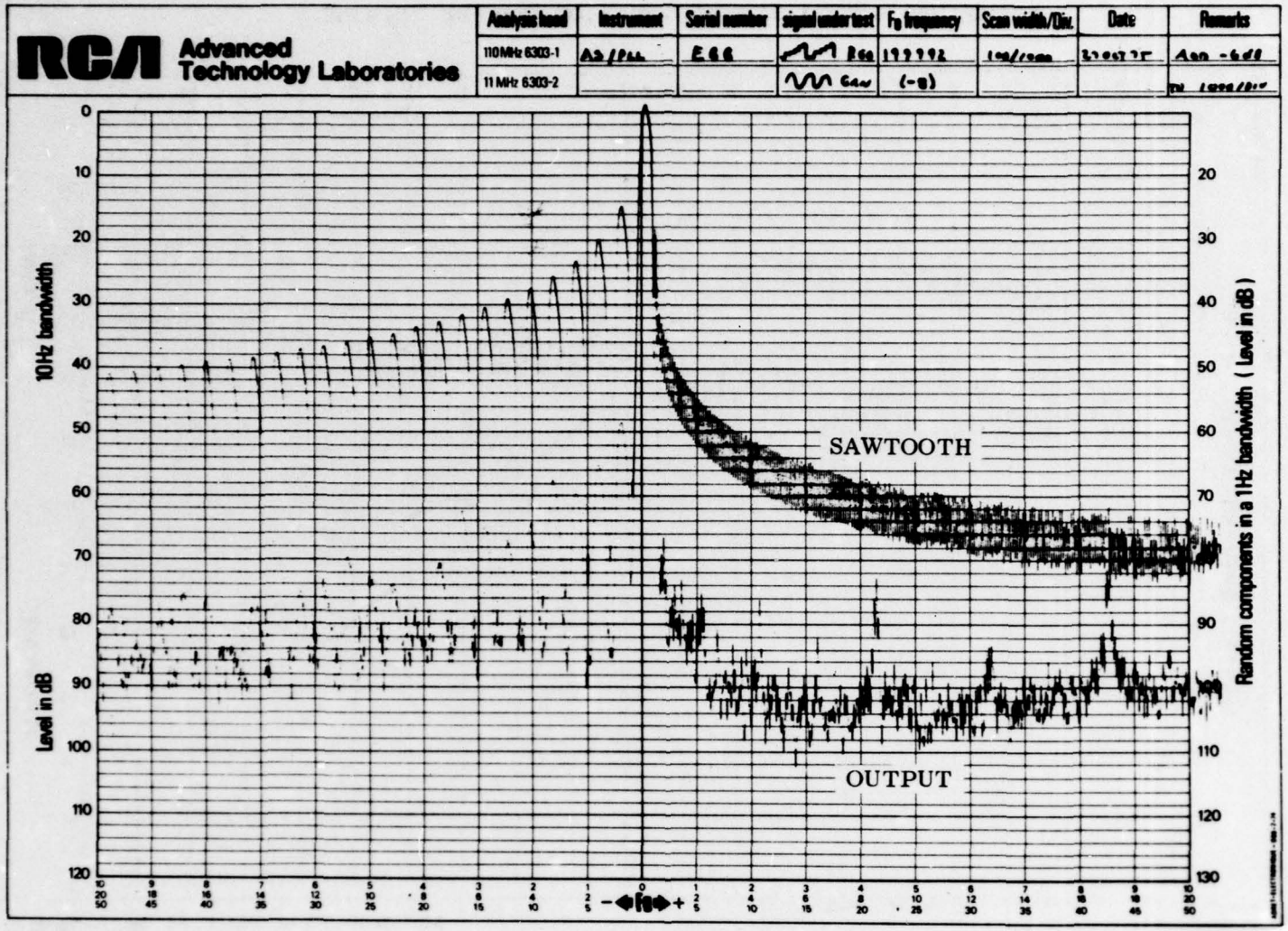


Figure 66. Sawtooth and output spectrum for f_o = 199, 992 Hz.

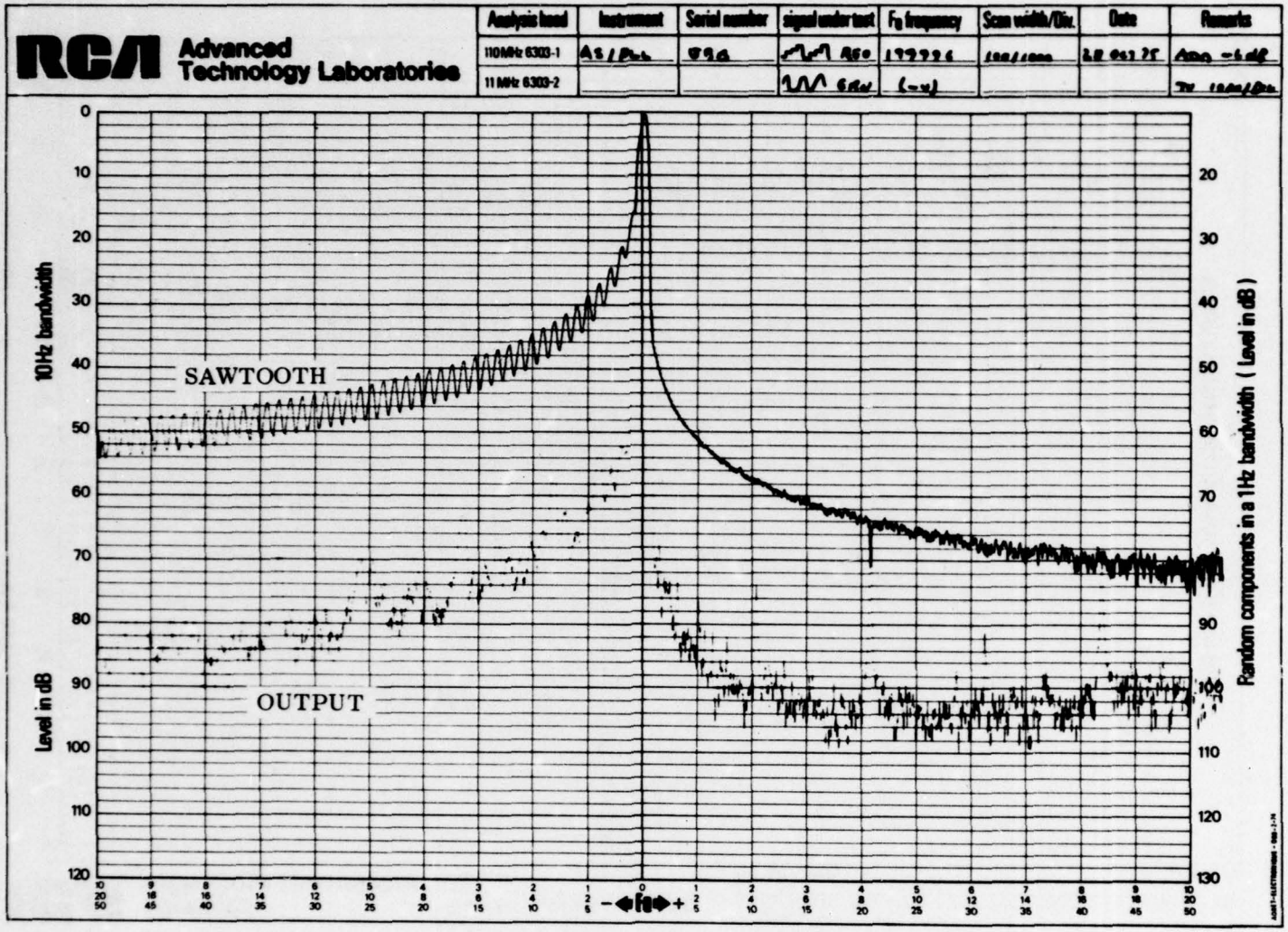


Figure 67. Sawtooth and output spectrum for f_o = 199,996 Hz.

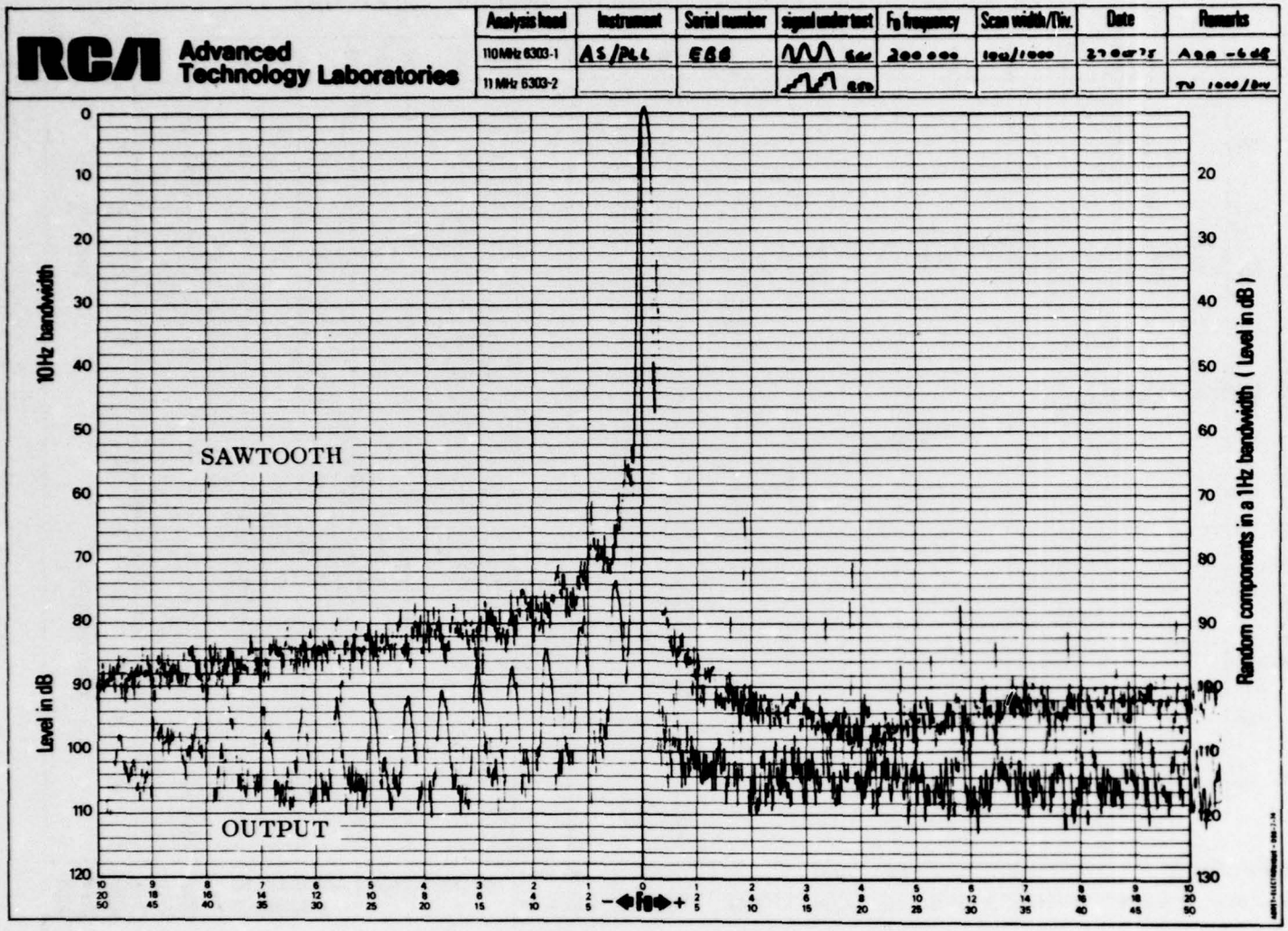
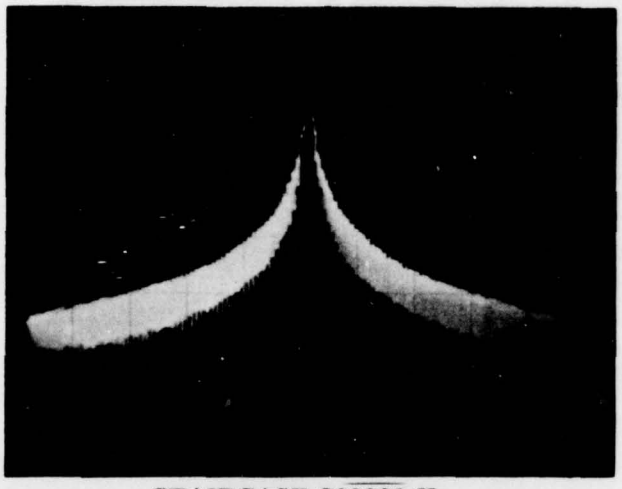
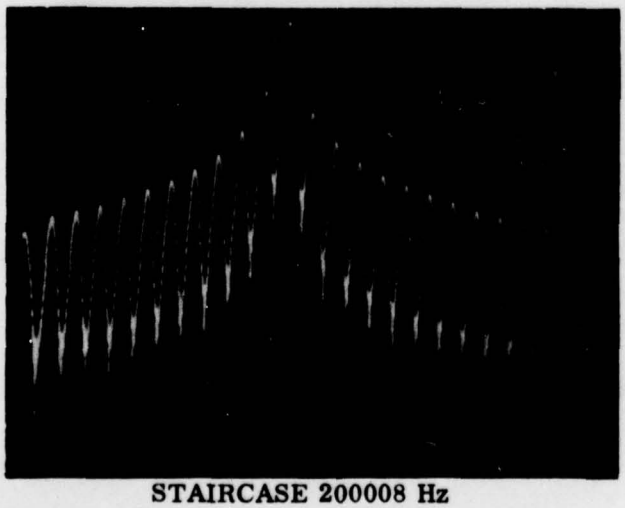


Figure 68. Sawtooth and output spectrum for f_o = 200,000 Hz.

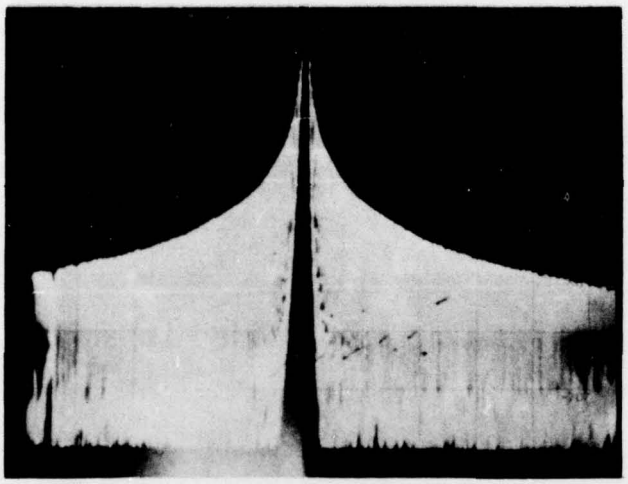


STAIRCASE 200008 Hz
1 KHz/DIV 30 Hz BW

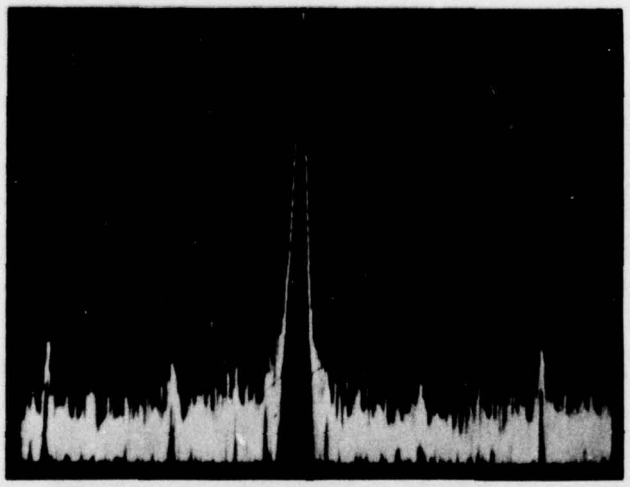


STAIRCASE 200008 Hz
100 Hz/DIV 10 Hz BW

Figure 69. Staircase spectrum using Hewlett-Packard analyzer, f_o = 200,008 Hz.



STAIRCASE 200008 Hz
2 KHz/DIV 100 Hz BW



PLL OUTPUT SINEWAVE 200008 Hz
2 KHz/DIV 100 Hz BW

Figure 70. Staircase and PLL output spectrum using Hewlett-Packard analyzer, f_o = 200, 008 Hz

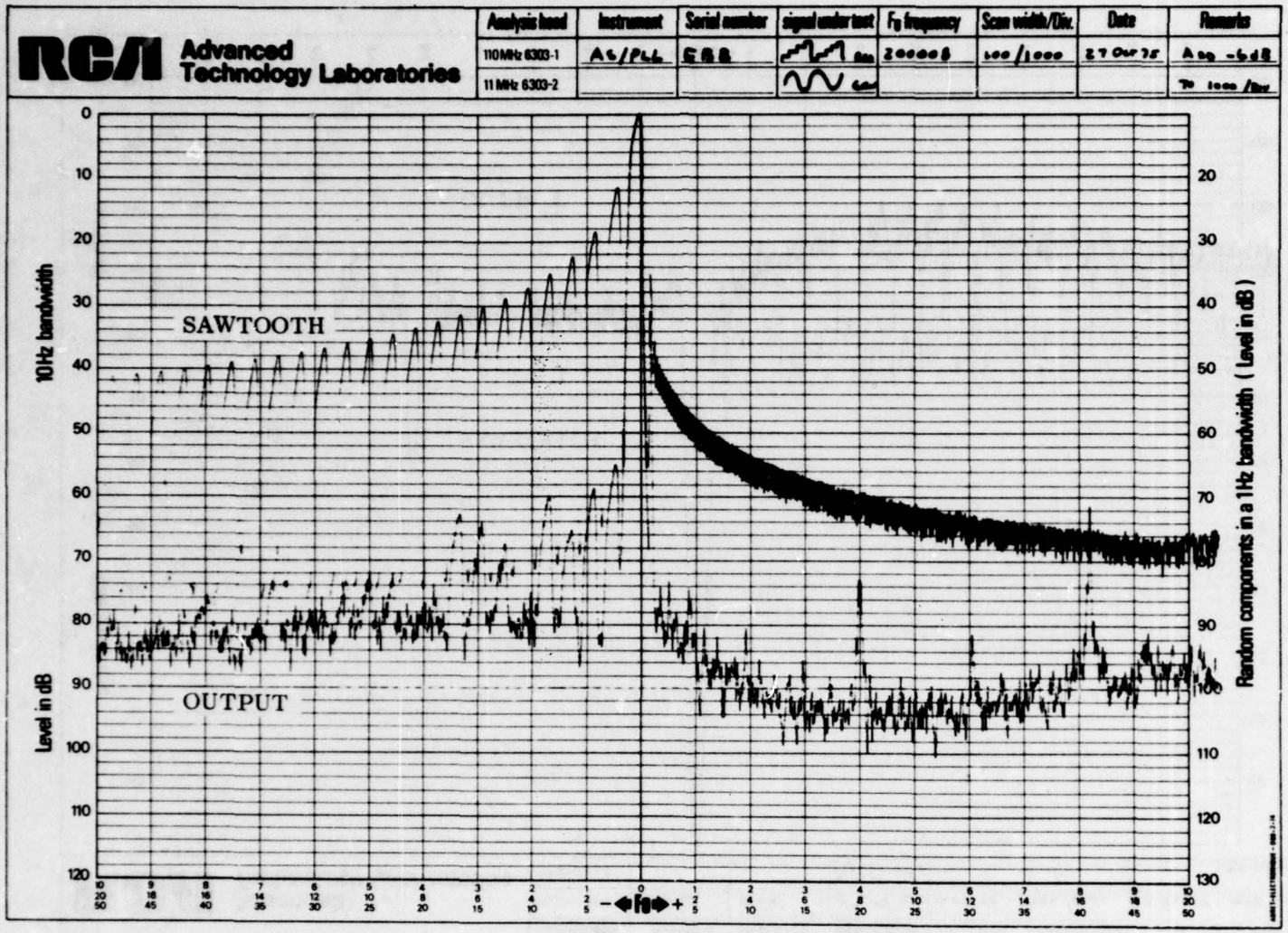


Figure 71. Sawtooth and output spectrum for f_o = 200, 008 Hz.

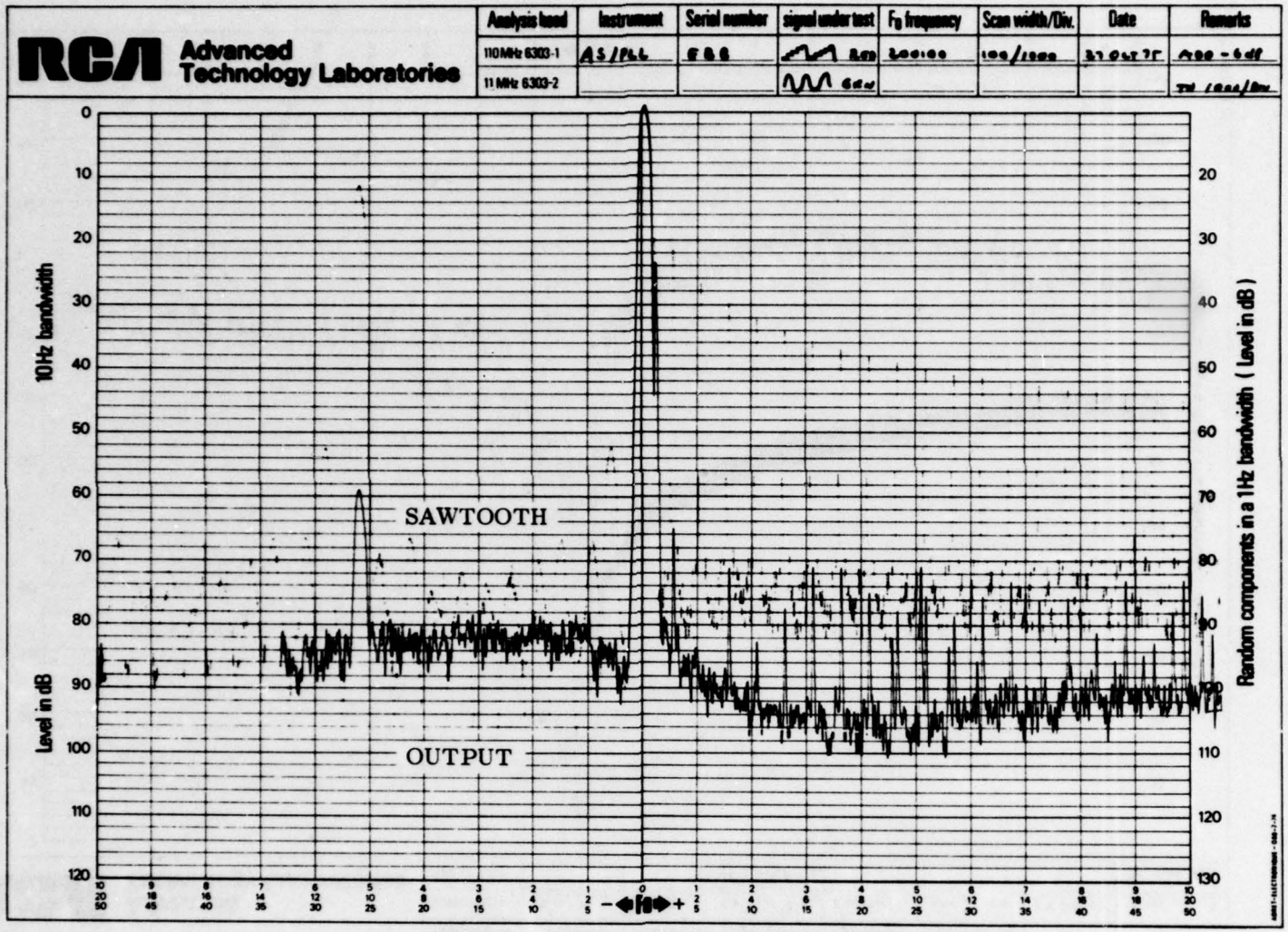


Figure 72. Sawtooth and output spectrum for f_o = 200, 100 Hz.

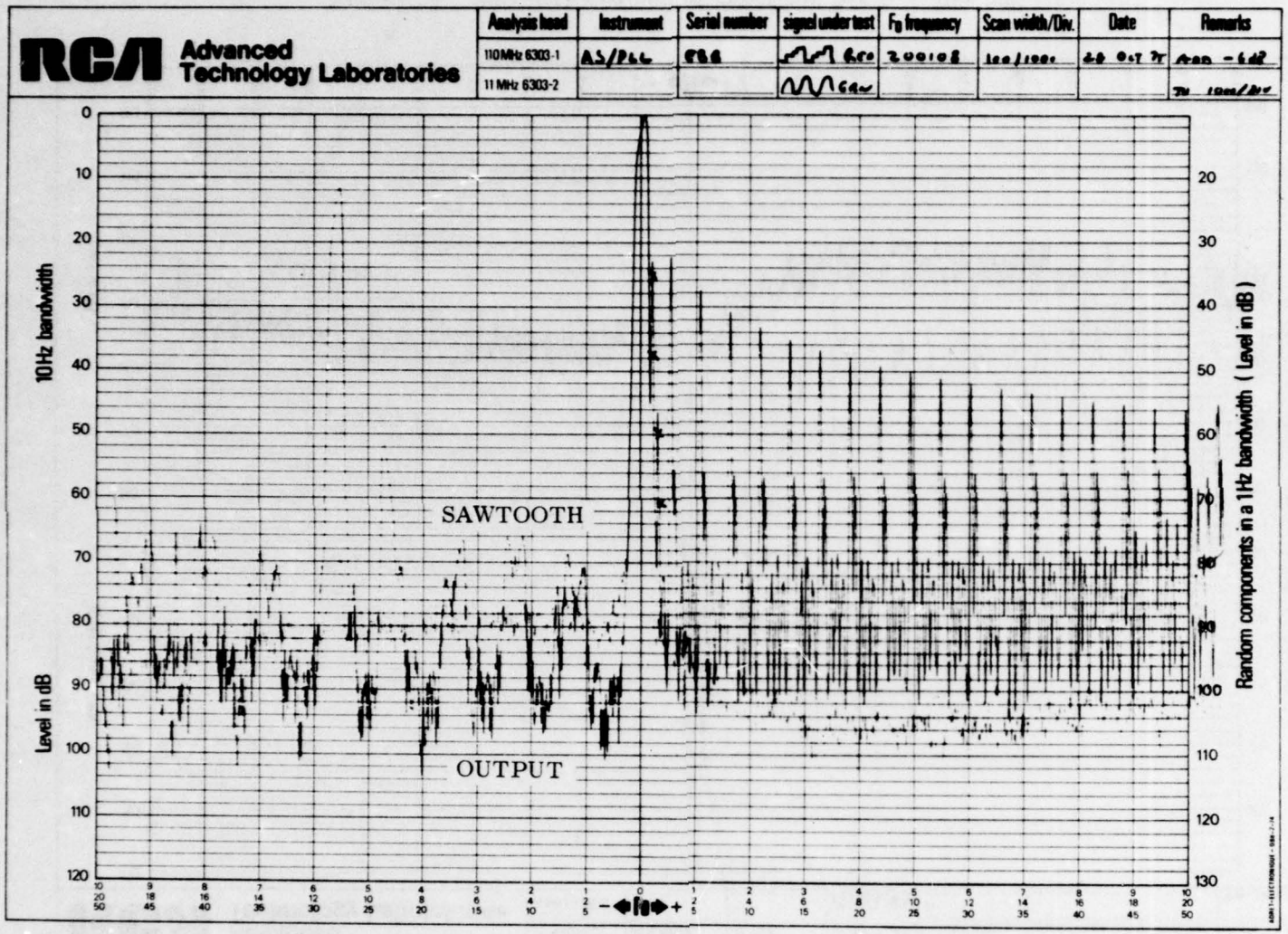


Figure 73. Sawtooth and output spectrum for f_o = 200,108 Hz.

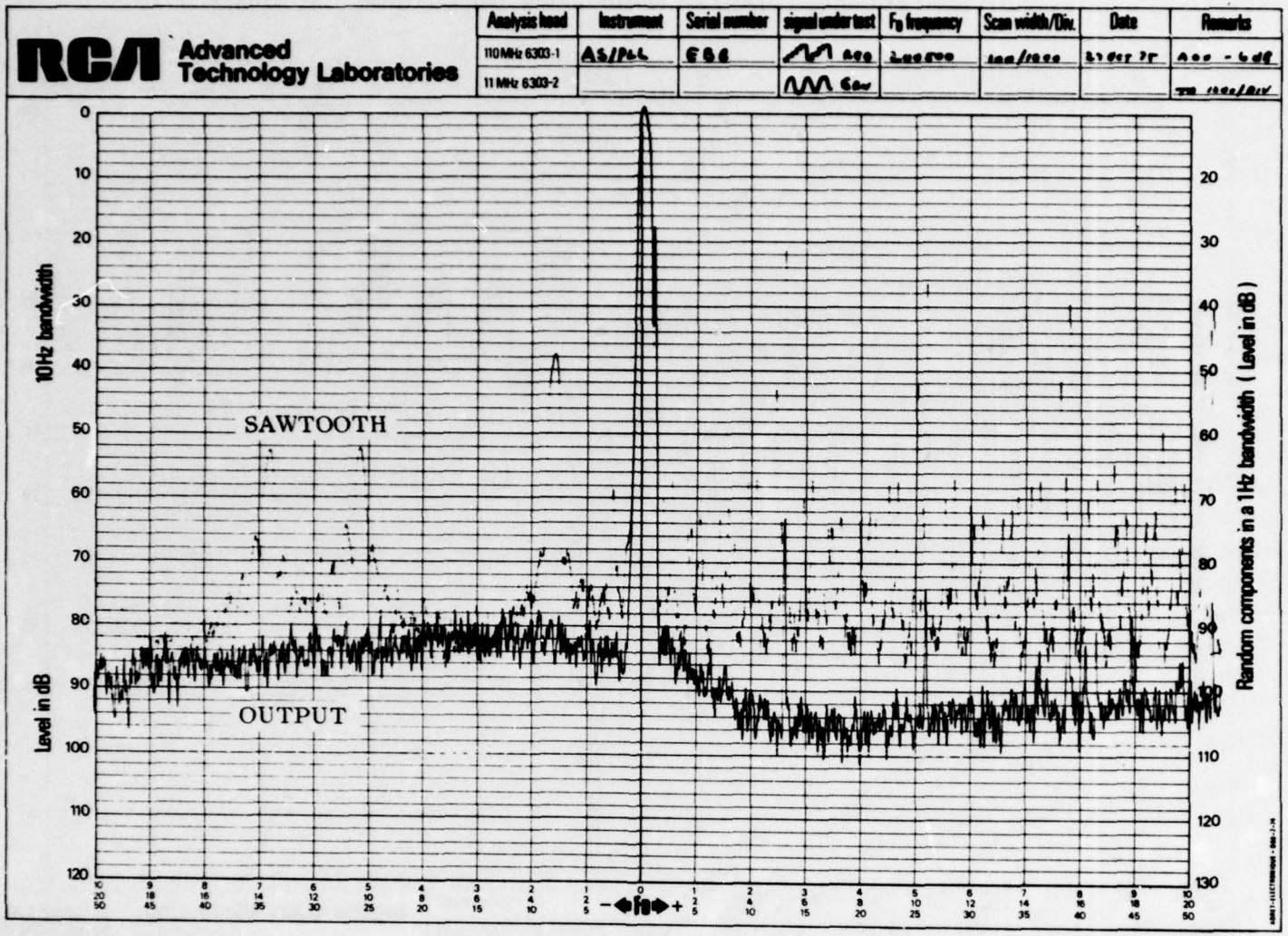


Figure 74. Sawtooth and output spectrum for f_0 = 200, 500 Hz.

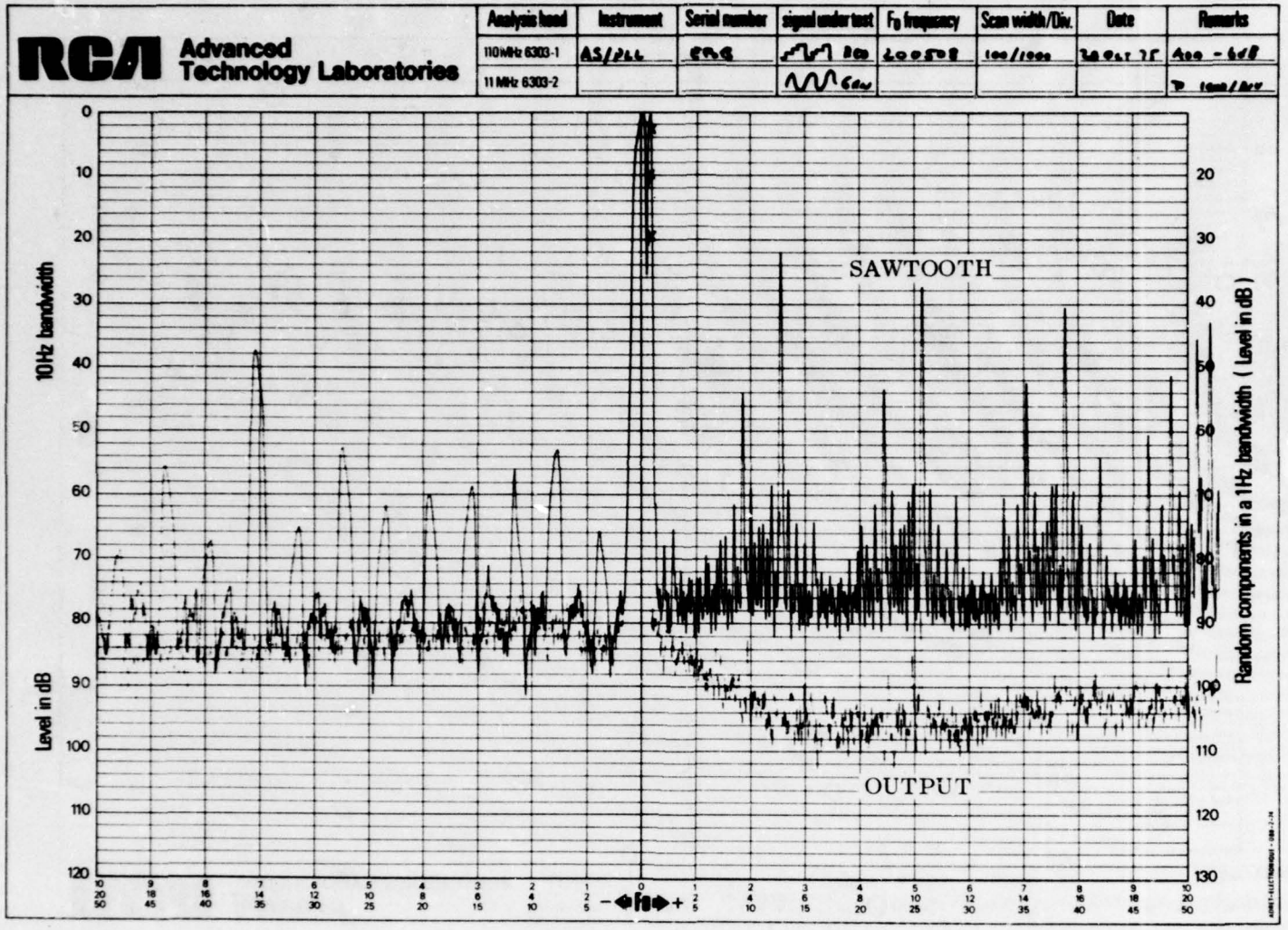


Figure 75. Sawtooth and output spectrum for f_o = 200, 508 Hz.

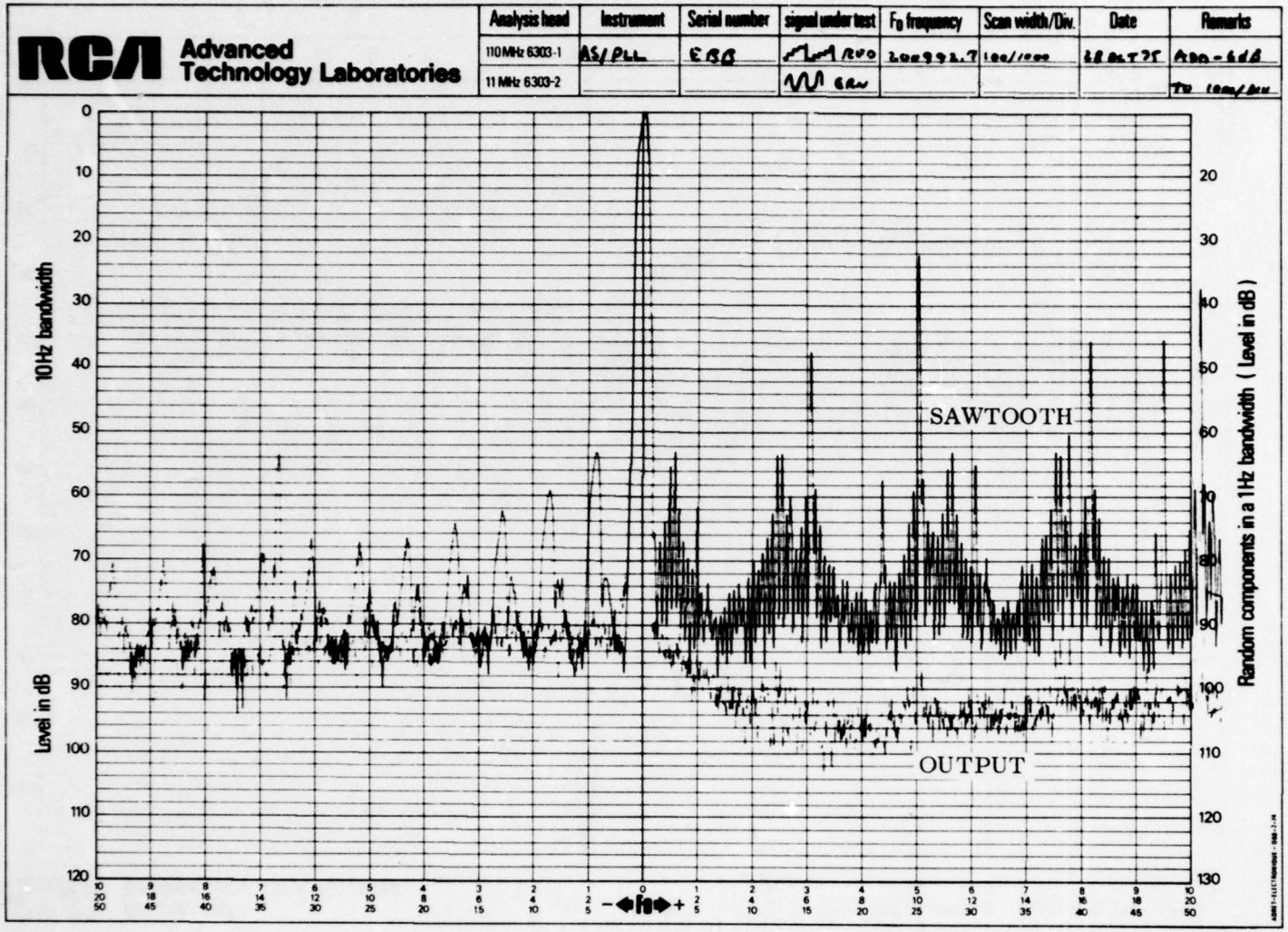


Figure 76. Sawtooth and output spectrum for f_o = 200, 992.7 Hz.

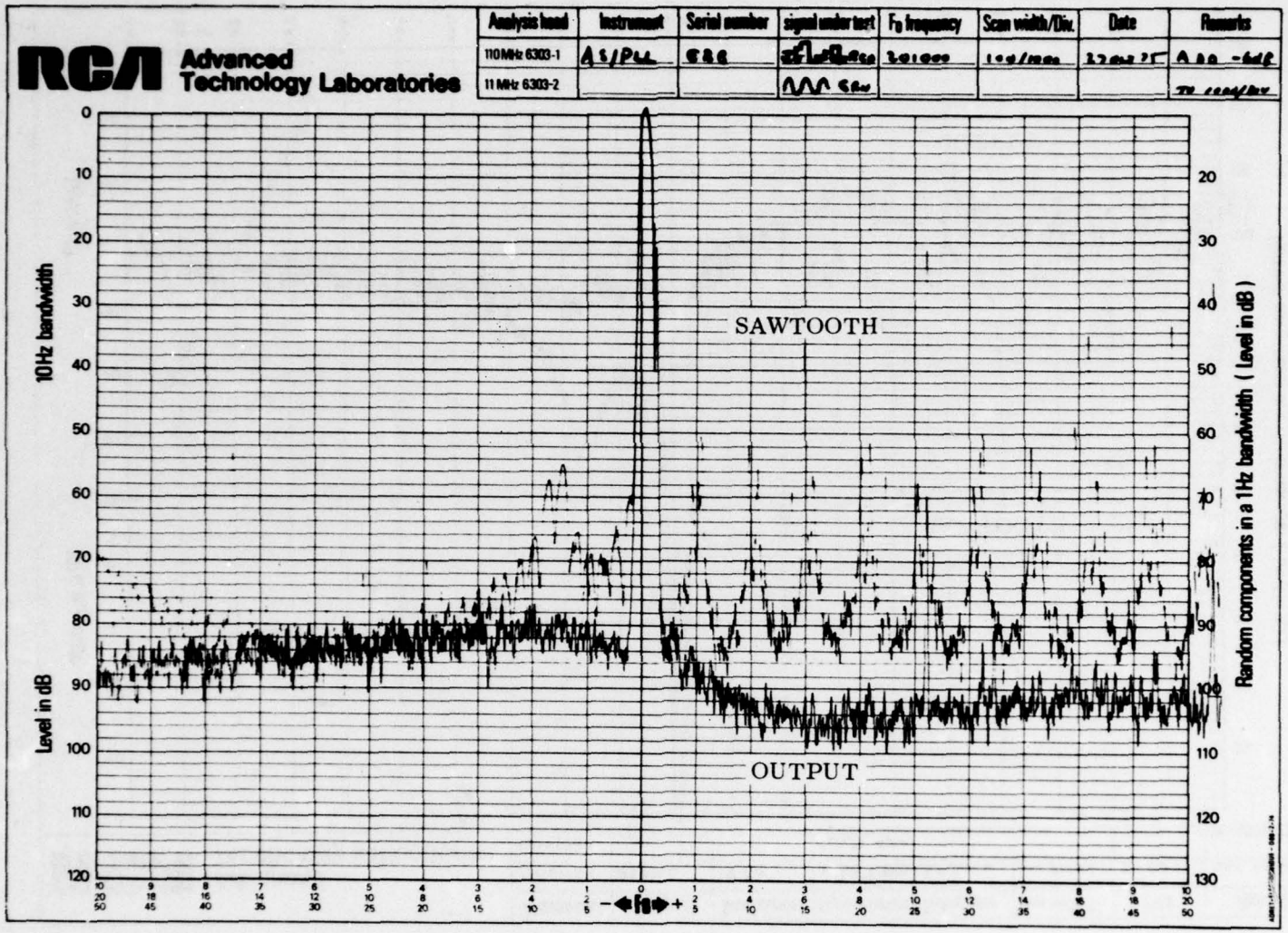


Figure 77. Sawtooth and output spectrum for f_o = 201,000 Hz.

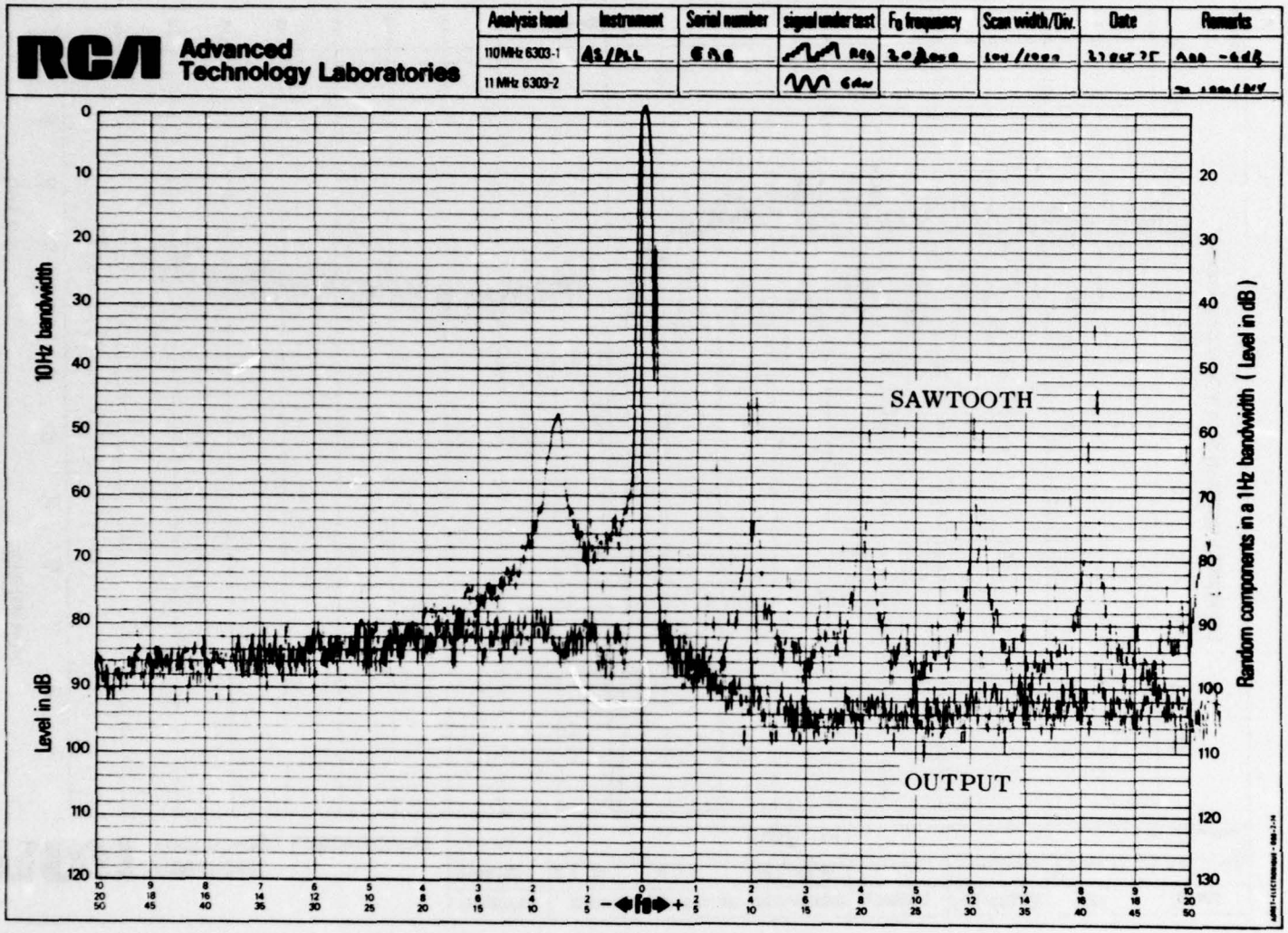
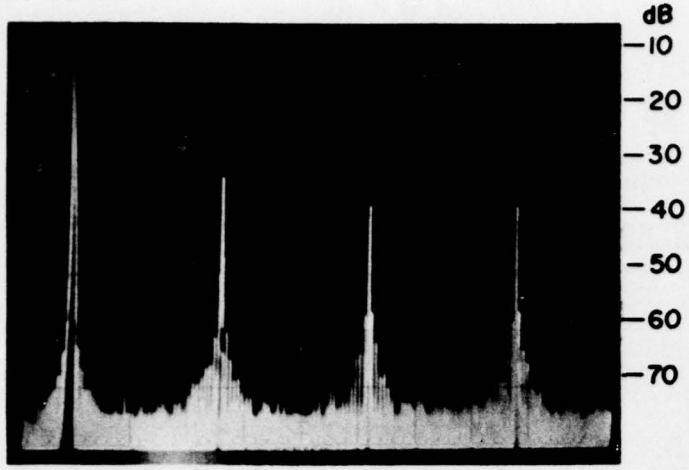
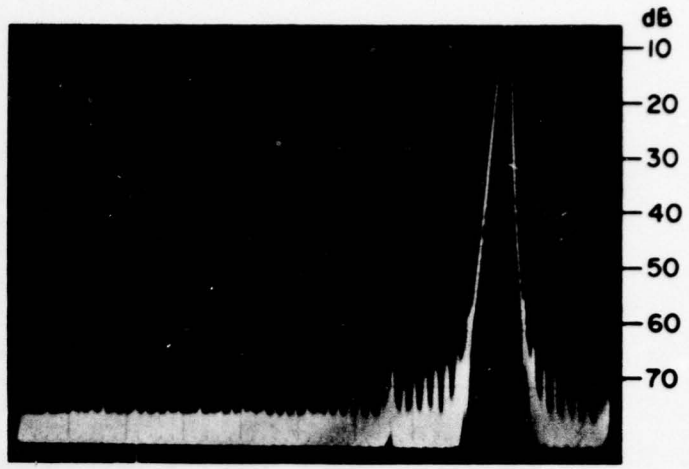


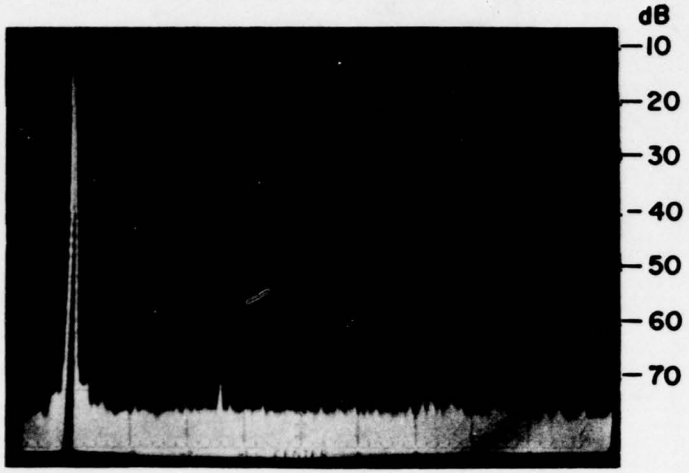
Figure 78. Sawtooth and output spectrum for f_o = 202,000 Hz.



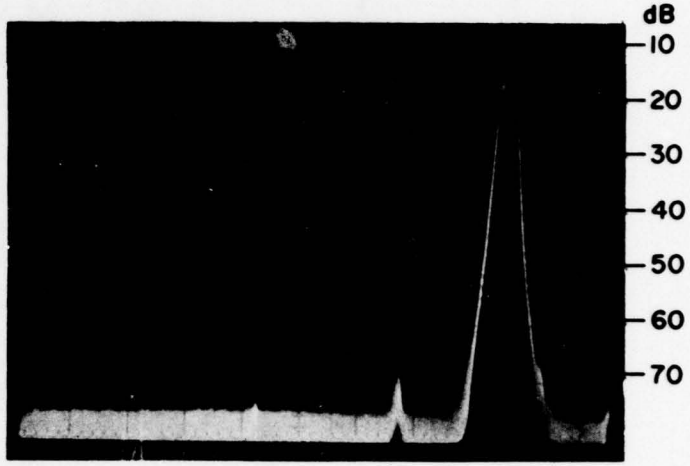
STAIRCASE 205000 Hz
2 kHz/DIV 300 Hz BW



STAIRCASE 205000 Hz
100 Hz/DIV 10 Hz BW



PLL OUTPUT SINEWAVE 205000 Hz
2 KHz/DIV 300 Hz BW



PLL OUTPUT SINEWAVE 205000 Hz
100 Hz/DIV 10 Hz BW

Figure 79. Staircase and PLL output spectrum, f_o = 205,000 Hz.

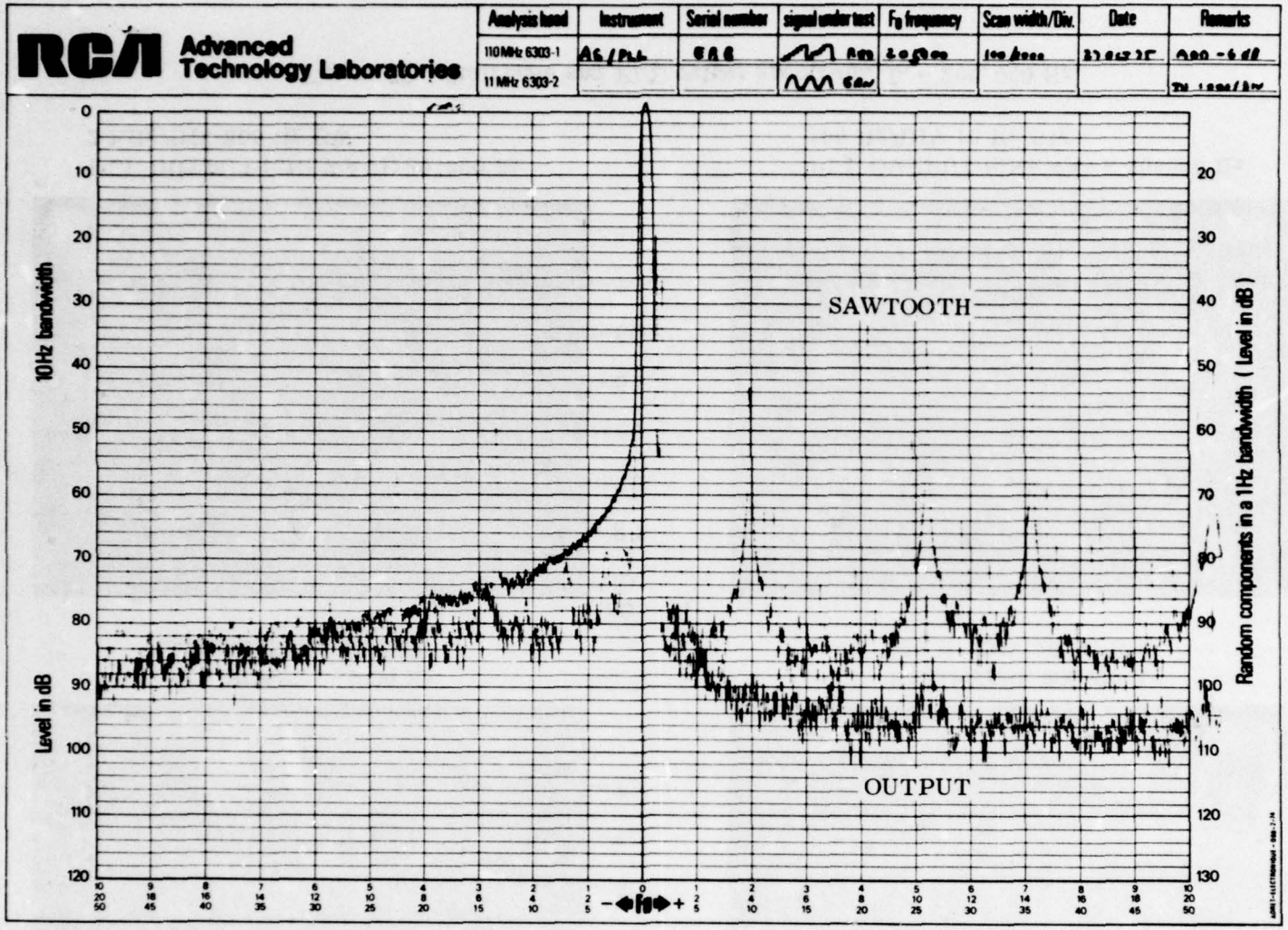


Figure 80. Sawtooth and output spectrum for f_o = 205,000 Hz.

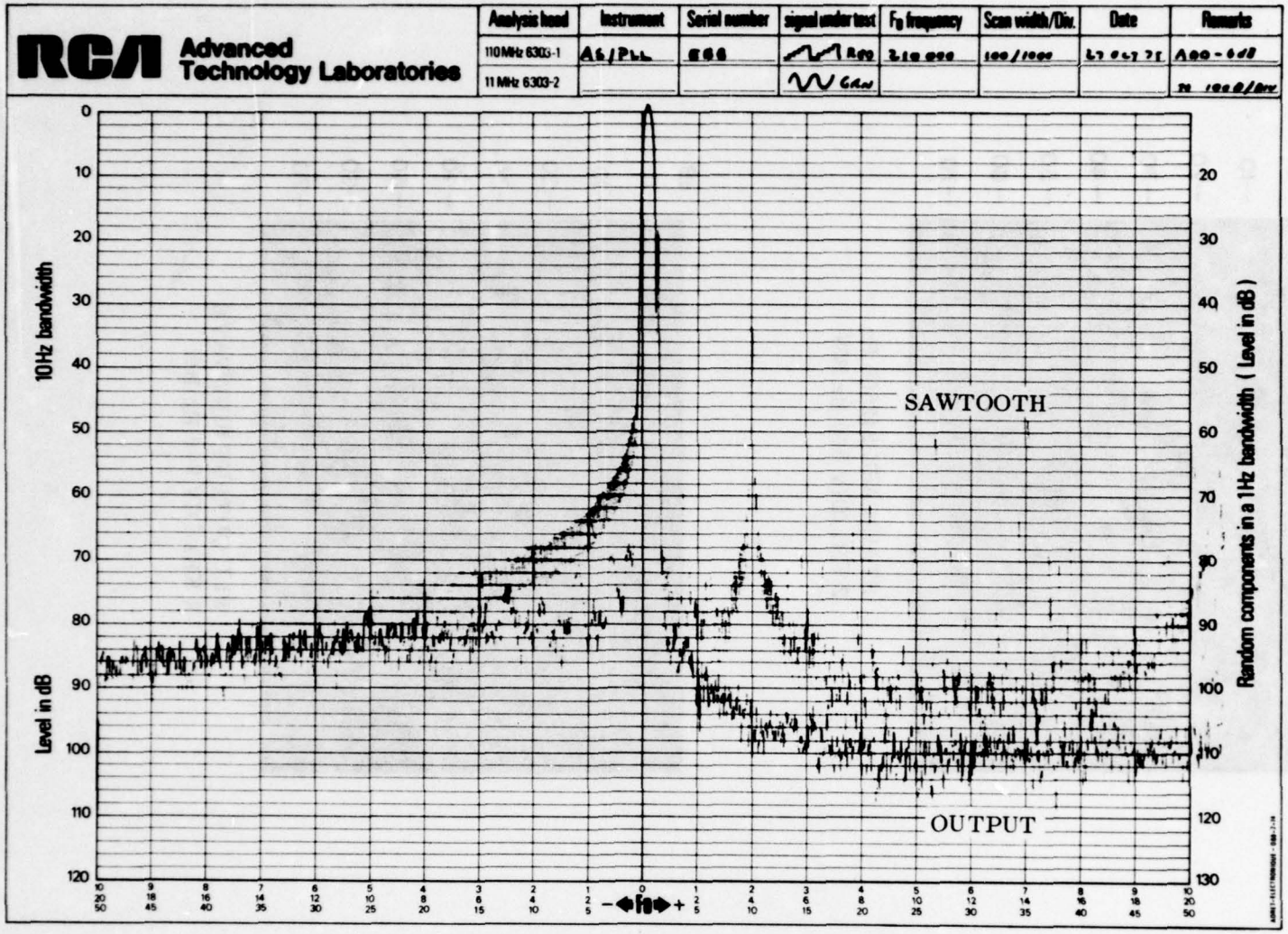
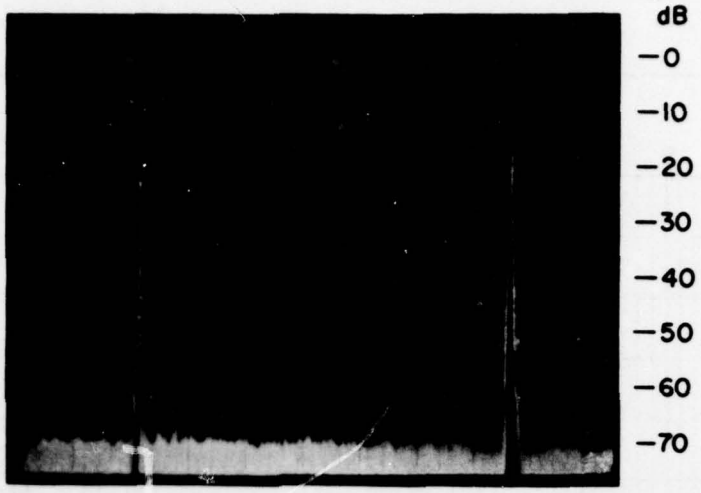
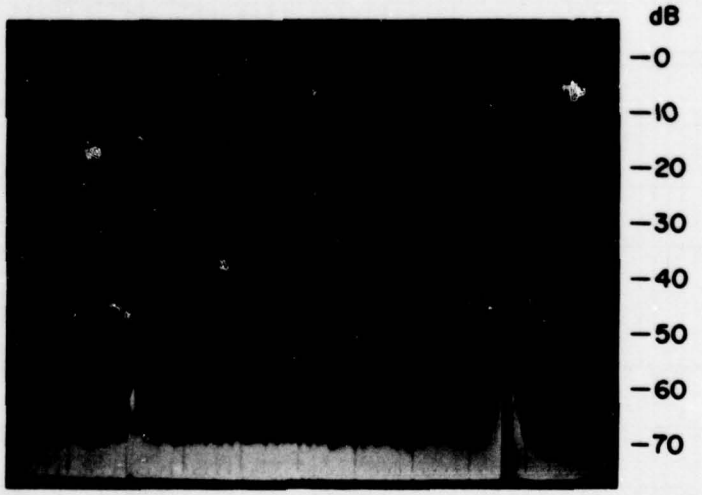


Figure 81. Sawtooth and output spectrum for f_o = 210,000 Hz.



STAIRCASE 212500 Hz
2 KHz/DIV 300 Hz BW



PLL OUTPUT SINEWAVE
2 KHz/DIV 300 Hz BW

Figure 82. Staircase and PLL output spectrum, f_o = 212, 500 Hz.

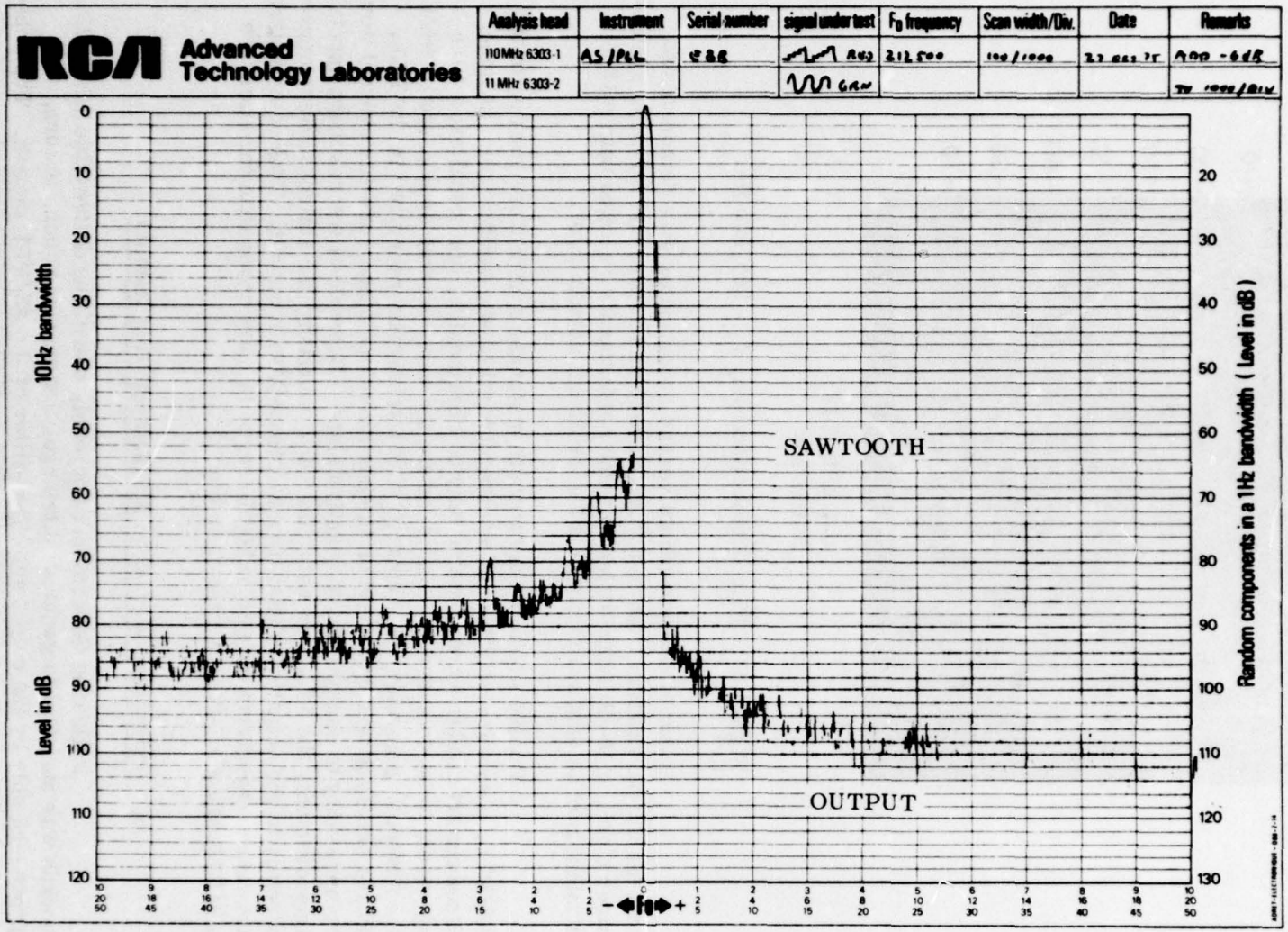
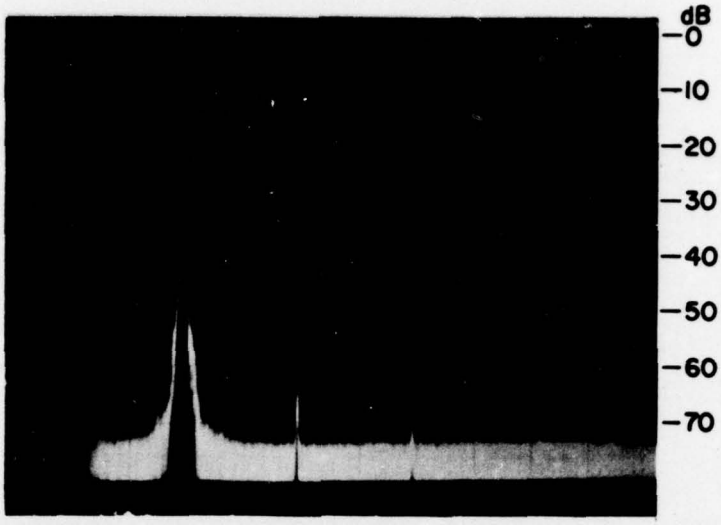


Figure 83. Sawtooth and output spectrum for f_o = 212, 500 Hz



0.1 MHz/DIV
3 KHz BW

Figure 84. PLL output spectrum, f_o = 200,000 Hz.

Spectral measurements versus accumulator size demonstrated that for the parameters used in the AS/PLL of this report and a 1-MHz synthesizer clock, a 10-dB degradation in noise performance resulted with a 16-bit accumulator as opposed to either a 24- or 32-bit accumulator.

During work on the sawtooth staircase synthesizer version of the AS/PLL, a side investigation of a triangular staircase synthesizer was done. Since the triangular wave contains only odd harmonics, one would expect the spectrum to be "cleaner." This is indeed the case and was demonstrated when the sawtooth generator was replaced with a triangular generator in the PLL. Phase sampling was done only on the positive slope since a phase reversal would be necessary to sample on the negative slope. Because of the resulting spectrum improvement, the PLL was eliminated and the triangular staircase was connected directly to the output amplifier-filter of the AS/PLL circuit. This combination produced a spectrum only 15 to 20 dB worse in most cases than the staircase AS/PLL using a 1-MHz synthesizer clock.

c. Triangular Waveform Synthesizer Test Results

Following Government approval, one of the deliverable AS/PLL boards was modified to generate a triangular staircase which, in turn, was processed only by the output amplifier-filter of the AS/PLL circuit. The schematic of this module, Figure 87, shows the elimination of the PLL.

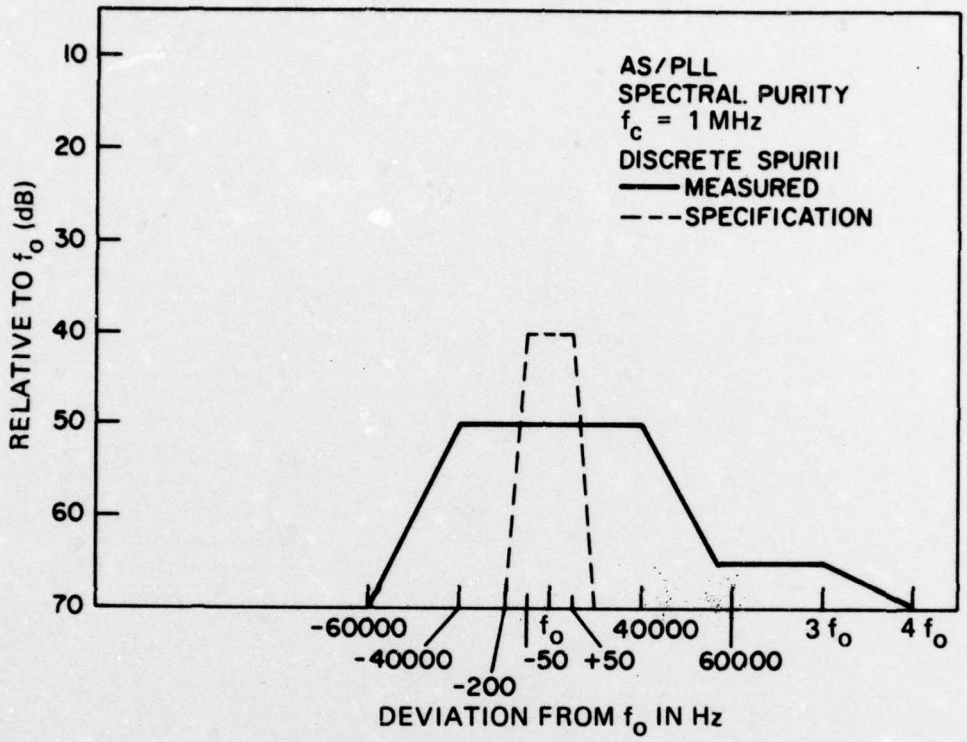


Figure 85. AS/PLL discrete spurii worst-case spectral limits.

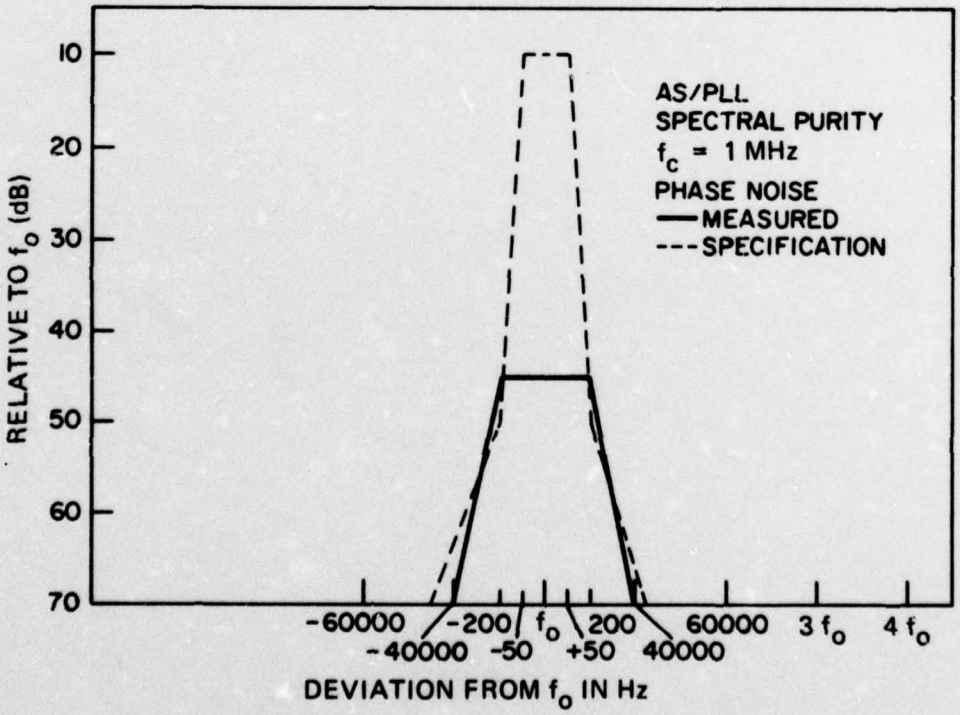
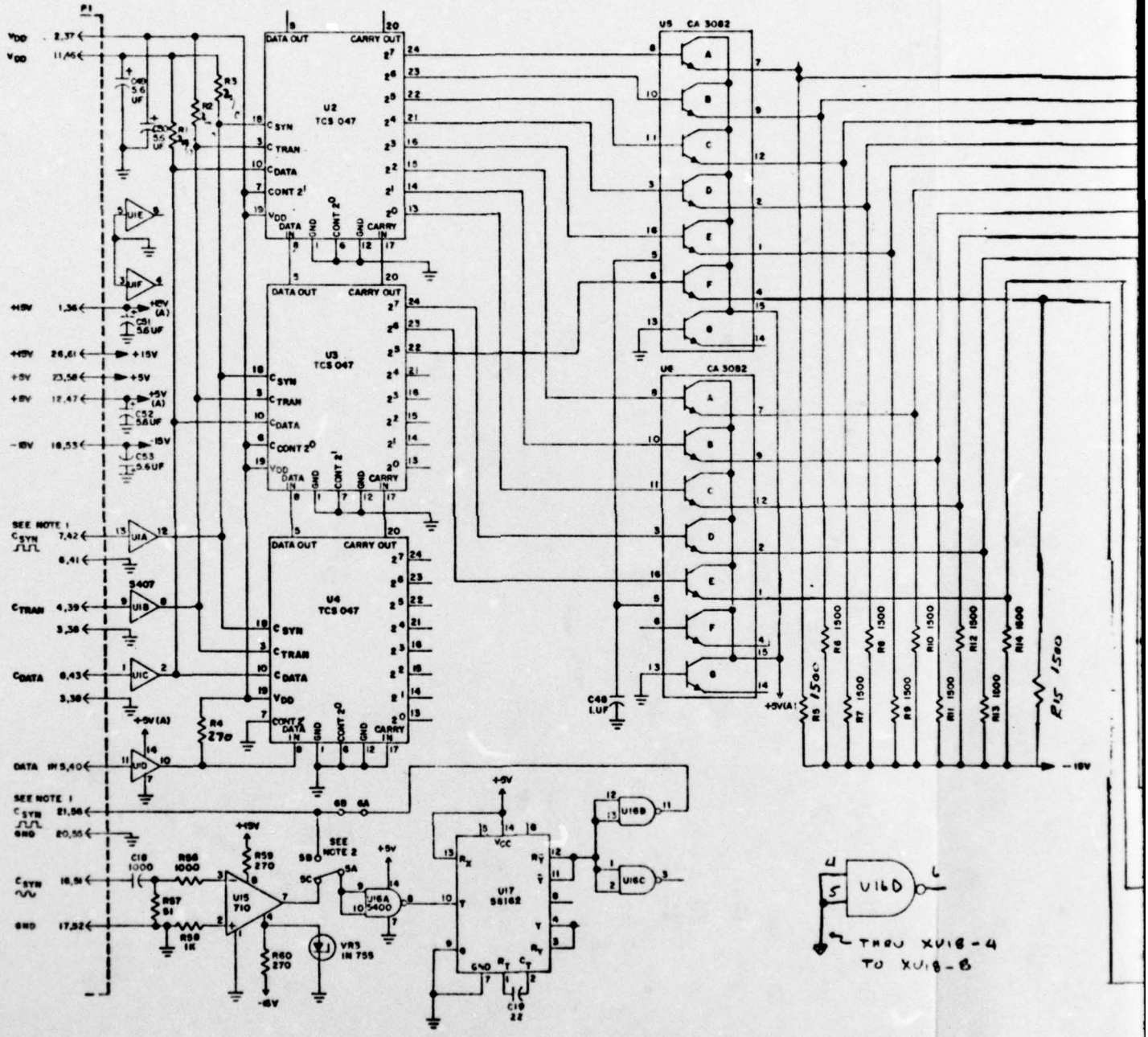
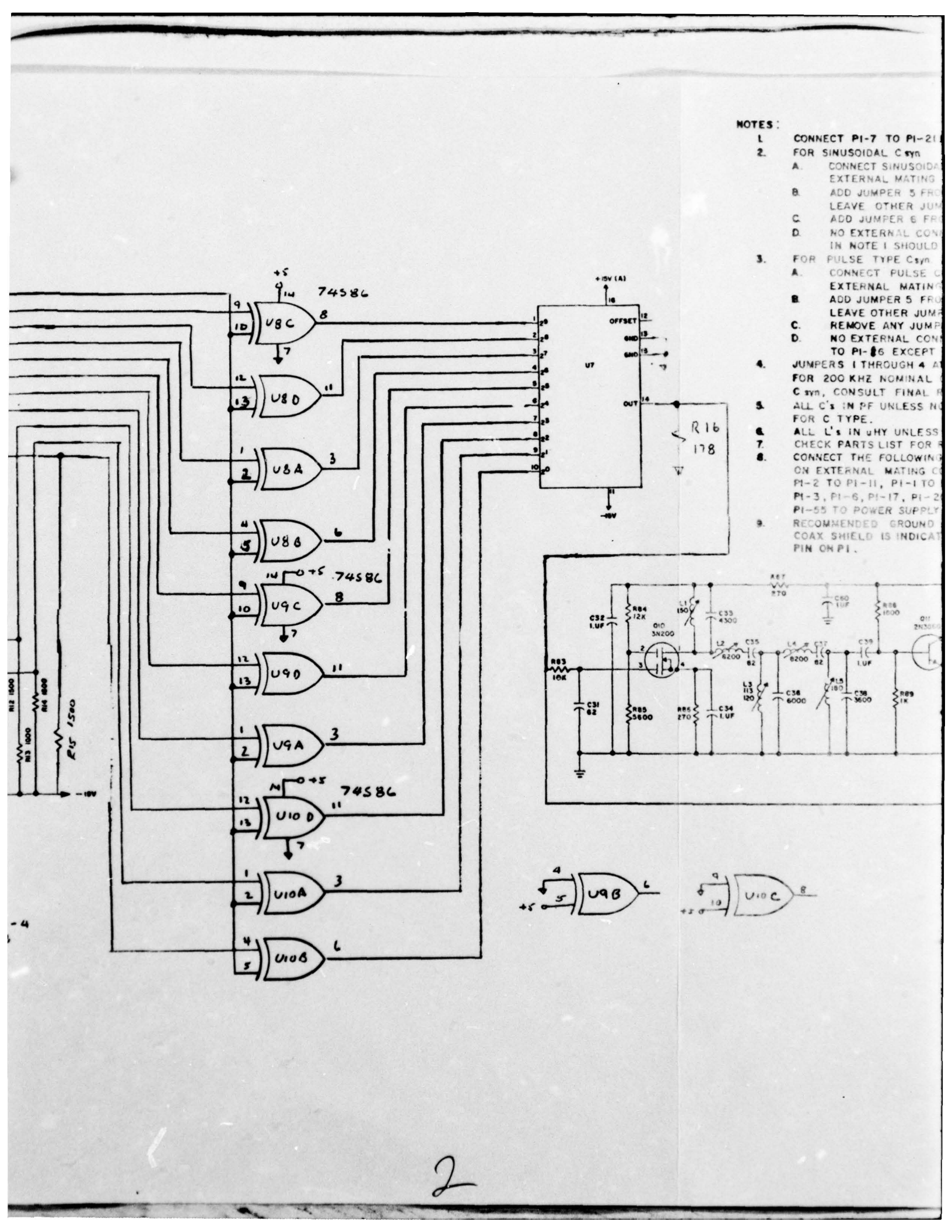


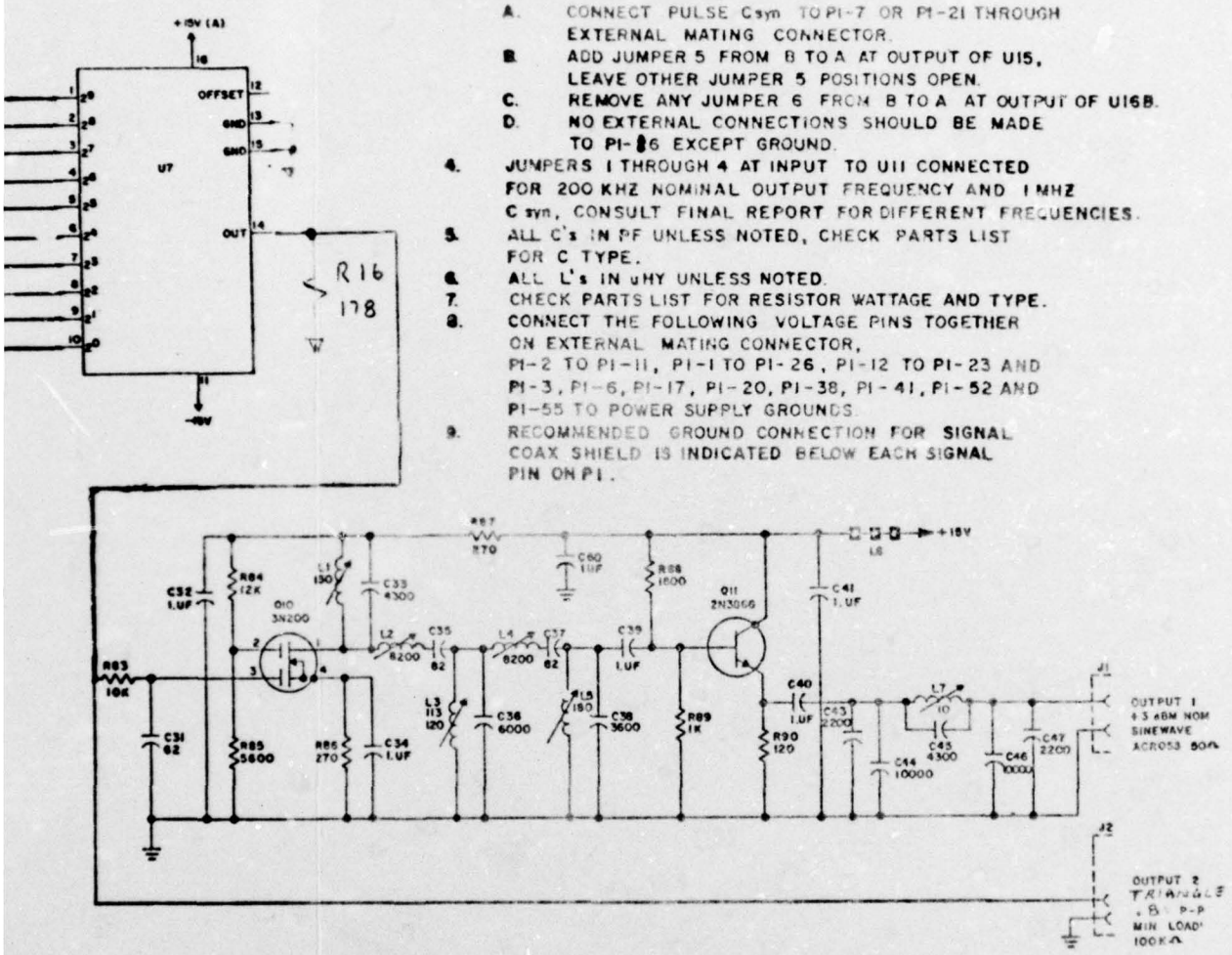
Figure 86. AS/PLL phase noise worst-case spectral limits.




NOTES:
1. CONNECT PI-7 TO PI-21
2. FOR SINUSOIDAL C syn
A. CONNECT SINUSOIDA
EXTERNAL MATING
B. ADD JUMPER 5 FR
LEAVE OTHER JUM
C. ADD JUMPER 6 FR
D. NO EXTERNAL CON
IN NOTE 1 SHOULD
3. FOR PULSE TYPE C syn
A. CONNECT PULSE
EXTERNAL MATIN
B. ADD JUMPER 5 FR
LEAVE OTHER JUM
C. REMOVE ANY JUMP
D. NO EXTERNAL CON
TO PI-36 EXCEPT
4. JUMPERS 1 THROUGH 4 A
FOR 200 KHZ NOMINAL
C syn, CONSULT FINAL
5. ALL C's IN PF UNLESS N
FOR C TYPE.
6. ALL L's IN uHY UNLESS
7. CHECK PARTS LIST FOR
8. CONNECT THE FOLLOWIN
ON EXTERNAL MATING C
PI-2 TO PI-11, PI-1 TO
PI-3, PI-6, PI-17, PI-2
PI-55 TO POWER SUPPLY
9. RECOMMENDED GROUND
COAX SHIELD IS INDICAT
PIN ON PI.
+5
74S86
U8C
U8D
U8A
U8B
U9C
U9D
U9A
U10D
U10A
U10B
U9B
U10C
+15V (A)
U7
OFFSET
GND
OUT
-15V
R16
178
R12 1500
R13 1000
R14 800
R15 1500
-15V
R84 12K
C32 1.UF
Q10 3N200
L1 150
C33 4300
L2 6200
C35 82
L4 6200
C37 82
C39 1.UF
R83 10K
C31 82
R85 5600
R86 270
C34 1.UF
L3 113 120
C36 6000
L5 180
C38 3600
R89 1K
R87 270
C40 1.UF
R88 1000
Q11 2N3906
- 4
2

NOTES:

1. CONNECT P1-7 TO P1-21 EXTERNALLY ON MATING CONNECTOR.
2. FOR SINUSOIDAL C syn
   - A. CONNECT SINUSOIDAL C syn TO P1-16 THROUGH EXTERNAL MATING CONNECTOR.
   - B. ADD JUMPER 5 FROM C TO A AT OUTPUT OF U15, LEAVE OTHER JUMPER 5 POSITIONS OPEN.
   - C. ADD JUMPER 6 FROM B TO A AT OUTPUT OF U16B.
   - D. NO EXTERNAL CONNECTIONS OTHER THAN JUMPER IN NOTE 1 SHOULD BE MADE TO P1-7 OR P1-21.
3. FOR PULSE TYPE C syn
   - A. CONNECT PULSE C syn TO P1-7 OR P1-21 THROUGH EXTERNAL MATING CONNECTOR.
   - B. ADD JUMPER 5 FROM B TO A AT OUTPUT OF U15, LEAVE OTHER JUMPER 5 POSITIONS OPEN.
   - C. REMOVE ANY JUMPER 6 FROM B TO A AT OUTPUT OF U16B.
   - D. NO EXTERNAL CONNECTIONS SHOULD BE MADE TO P1-36 EXCEPT GROUND.
4. JUMPERS 1 THROUGH 4 AT INPUT TO U11 CONNECTED FOR 200 KHZ NOMINAL OUTPUT FREQUENCY AND 1 MHZ C syn, CONSULT FINAL REPORT FOR DIFFERENT FREQUENCIES.
5. ALL C's IN PF UNLESS NOTED, CHECK PARTS LIST FOR C TYPE.
6. ALL L's IN uHY UNLESS NOTED.
7. CHECK PARTS LIST FOR RESISTOR WATTAGE AND TYPE.
8. CONNECT THE FOLLOWING VOLTAGE PINS TOGETHER ON EXTERNAL MATING CONNECTOR, P1-2 TO P1-11, P1-1 TO P1-26, P1-12 TO P1-23 AND P1-3, P1-6, P1-17, P1-20, P1-38, P1-41, P1-52 AND P1-55 TO POWER SUPPLY GROUNDS.
9. RECOMMENDED GROUND CONNECTION FOR SIGNAL COAX SHIELD IS INDICATED BELOW EACH SIGNAL PIN ON P1.



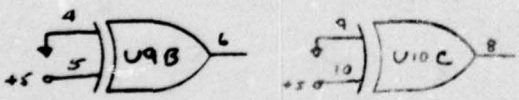


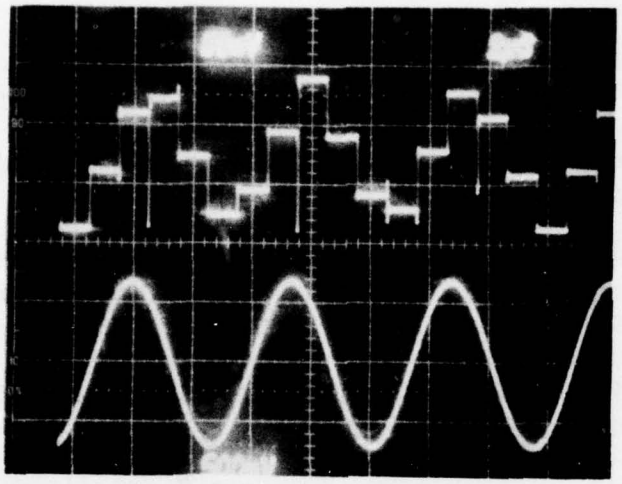
Figure 87. Triangle waveform arithmetic synthesizer schematic.

3

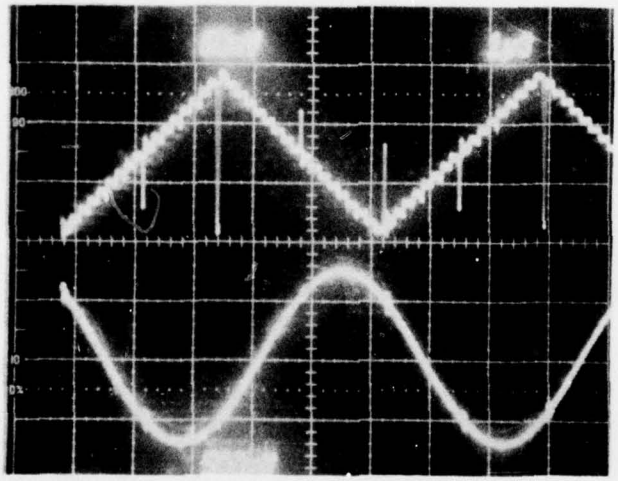
Figure 88 shows the circuit waveforms for a 1 MHz and 6.4 MHz clock for a 187.5 kHz triangular waveform AS and corresponding output sine wave. Since a delayed sample pulse is not needed, the input clock freaquency is limited primarily by the DAC, the TTL clock circuitry and the CMOS/TTL level translation circuitry.

Spectral responses of this module using a 1-MHz clock are given in Figures 89 through 100. Comparison of these figures with the corresponding frequency for the AS/PLL of Figures 59 through 84 shows that, in general, the phase noise is 20 to 30 dB lower for the triangular waveform while the discrete close-in spurii are 10 to 30 dB higher. (Spuriii at 60 Hz, 120 Hz and 180 Hz are test equipment ground loop signals.)

The unsymmetrical spectrum of the triangular wave synthesizer sinewave output (spectrum photos) contrasts with the symmetrical spectrum of the staircase synthesizer sine wave. This attests to the high linearity of the DAC and output amplifier circuitry, thus indicating that most of the spurii are generated within the portion of the PLL circuitry dedicated to phase control. As stated previously, nonlinearities here would enhance or generate spurii and also produce symmetrical sidebands from an unsymmetrical sideband spectrum.



TRIANGLE AS - 1 MHz CLOCK
FREQ. = 187.5 KHz
UPPER: DAC OUTPUT
LOWER: FILTER/AMPL. OUTPUT



TRIANGLE AS - 6.4 MHz CLOCK
FREQ. = 187.5 KHz
UPPER: DAC OUTPUT
LOWER: FILTER/AMPL. OUTPUT

Figure 88. Circuit waveforms using a 1-MHz and 6.4-MHz clock for a 187.5-kHz triangular waveform AS and corresponding output sine wave.

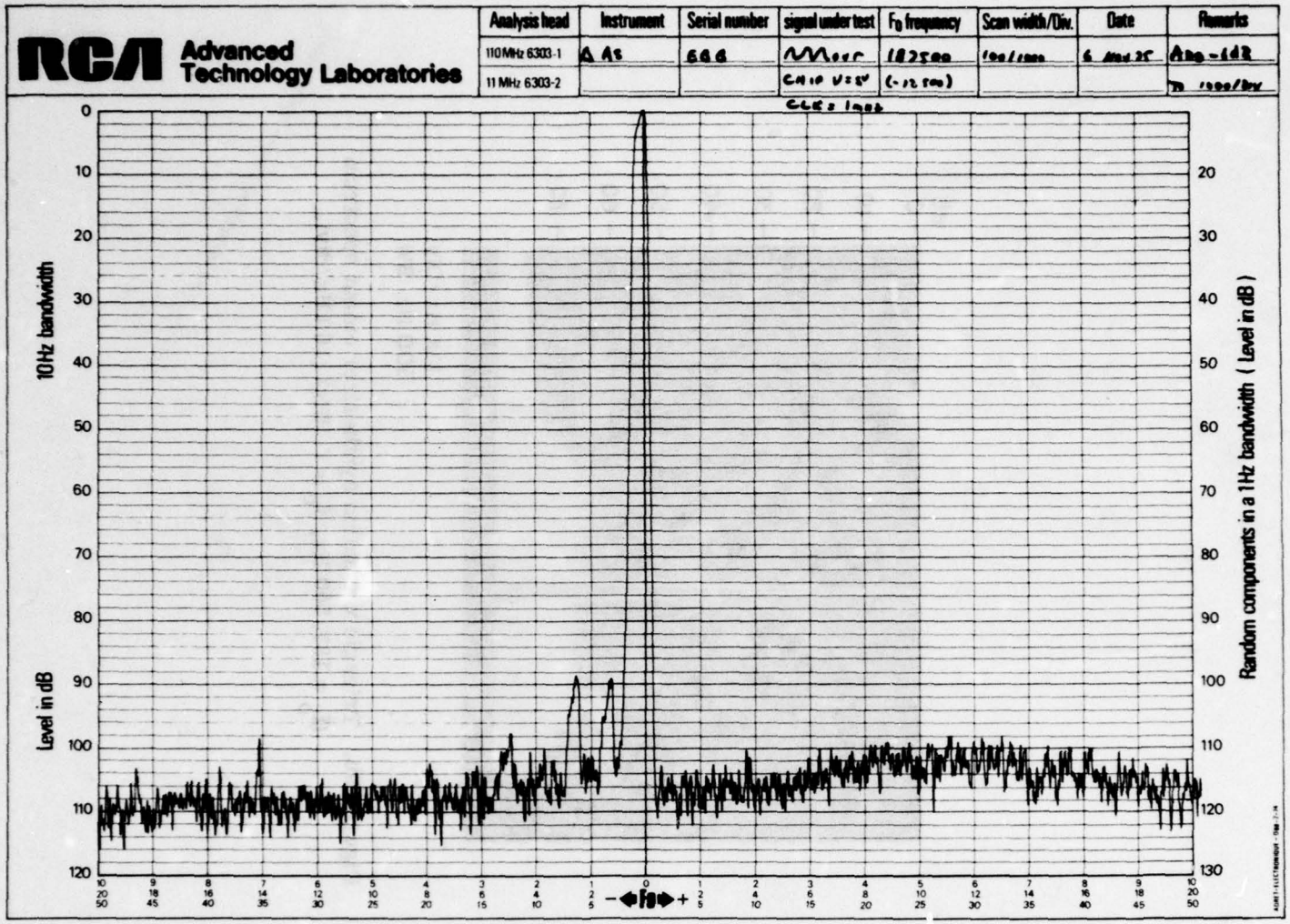


Figure 89a. Triangle waveform synthesizer output spectrum (f_o = 187,500 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

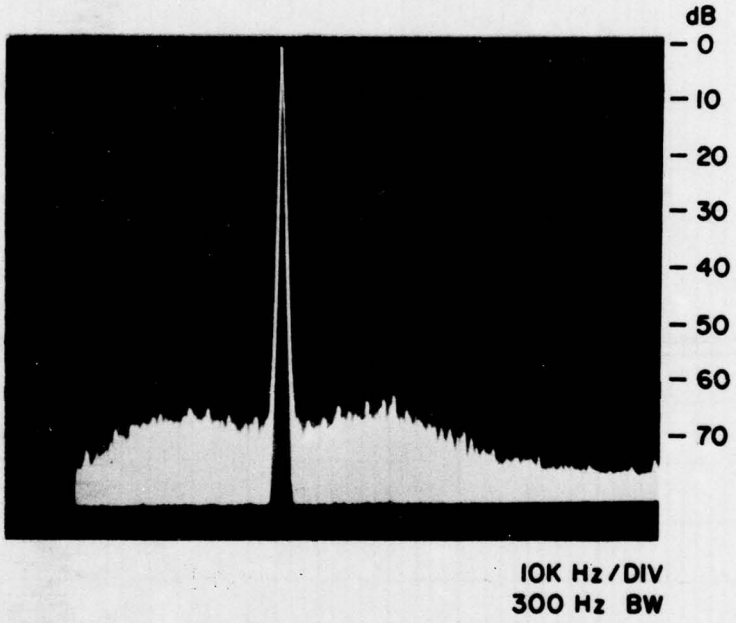


Figure 89b. Triangle waveform synthesizer output spectrum (f_o = 187, 500 Hz, f_c = 1 MHz) (10 kHz/div)..

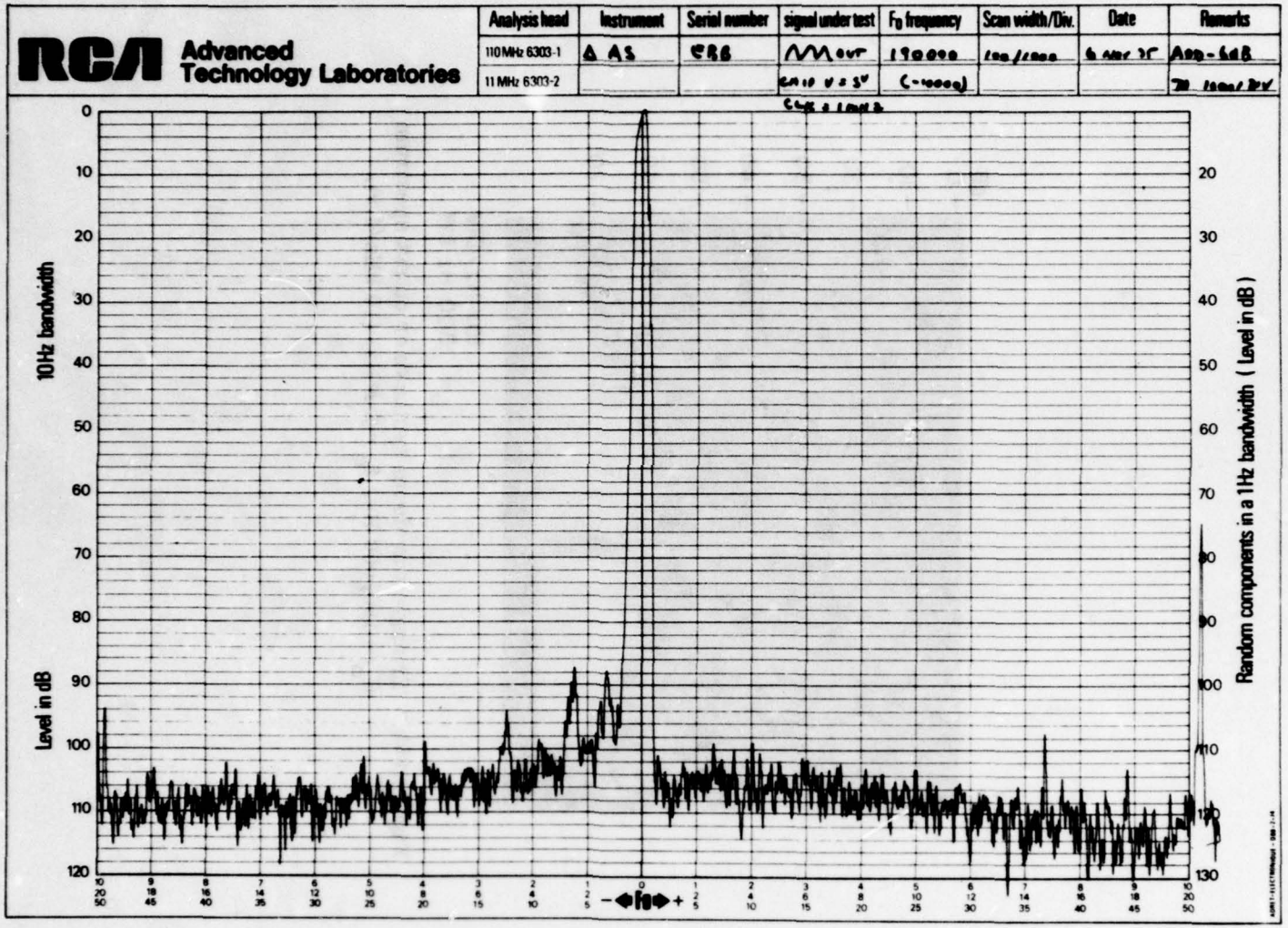


Figure 90a. Triangle waveform synthesizer output spectrum (f_o = 190,000 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

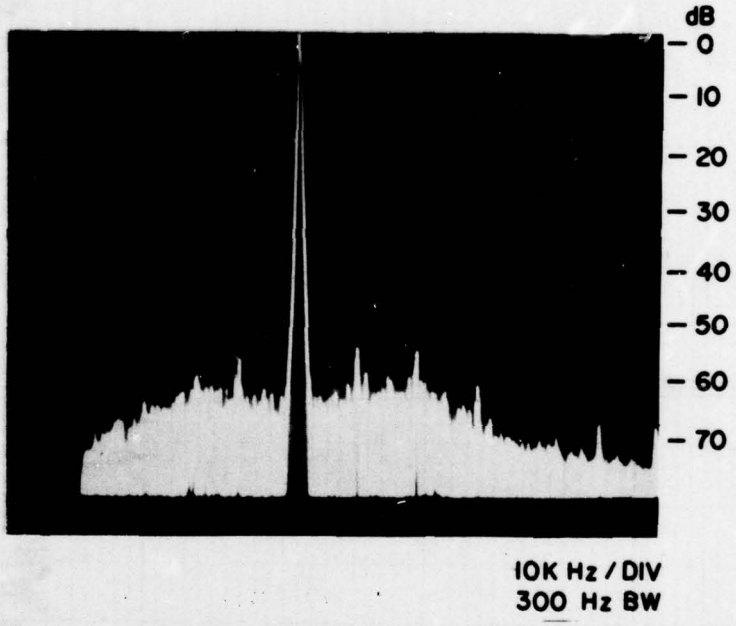


Figure 90b. Triangle waveform synthesizer output spectrum (f_o = 190, 000 Hz, f_c = 1 MHz) (10 kHz/div).

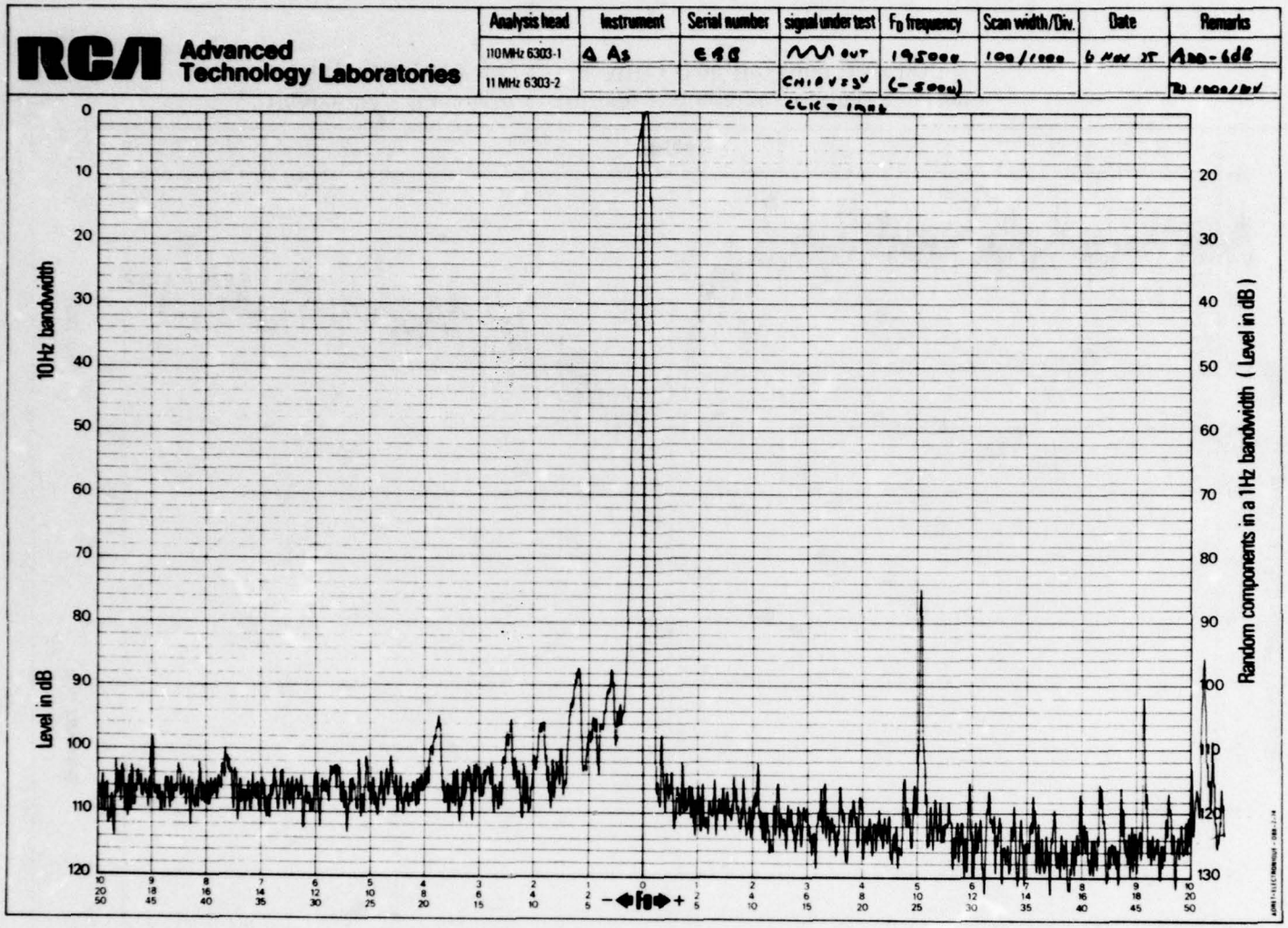


Figure 91. Triangle waveform synthesizer output spectrum (f_o = 195,000 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

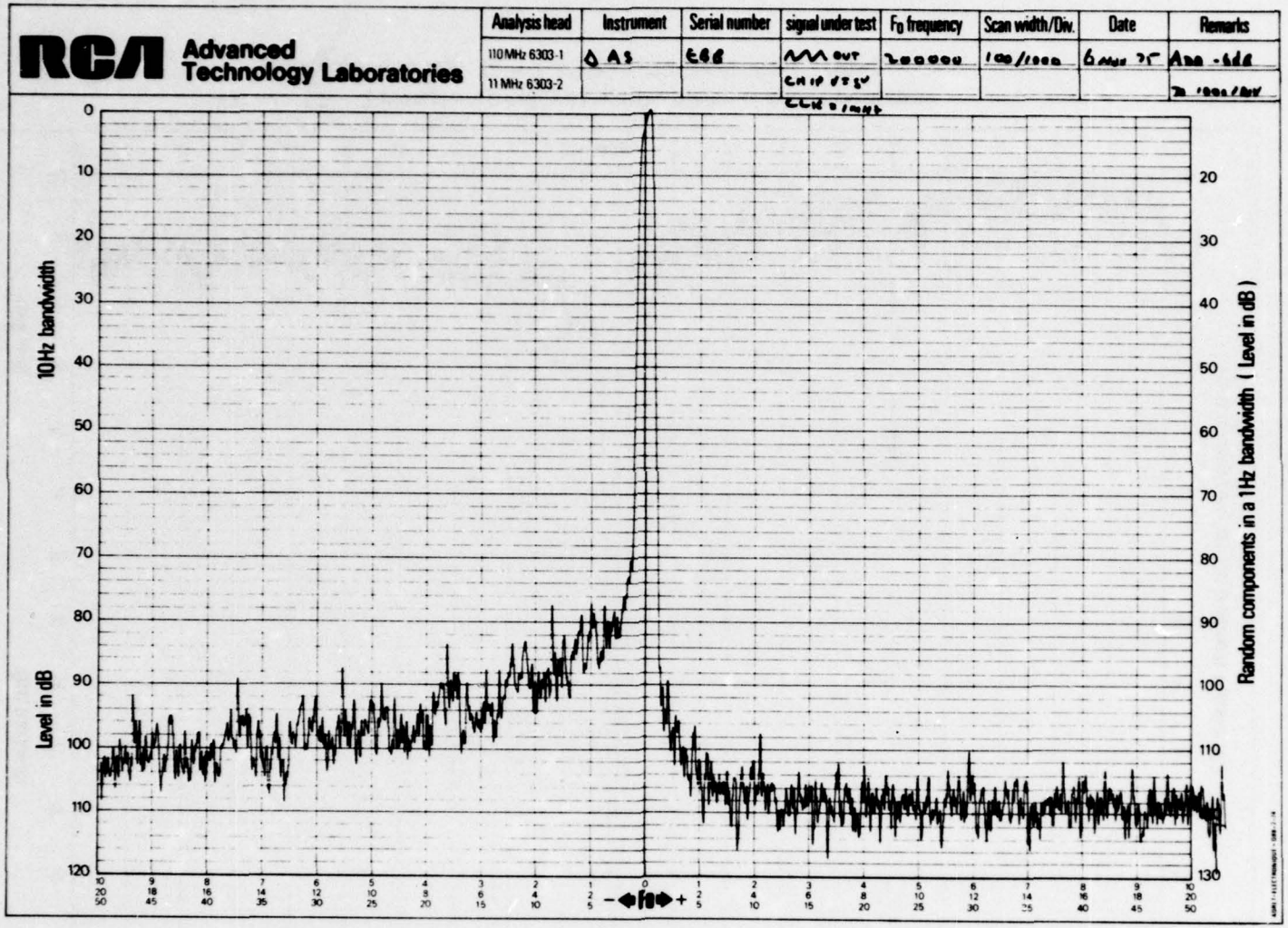


Figure 92. Triangle waveform synthesizer output spectrum (f_o = 200,000 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

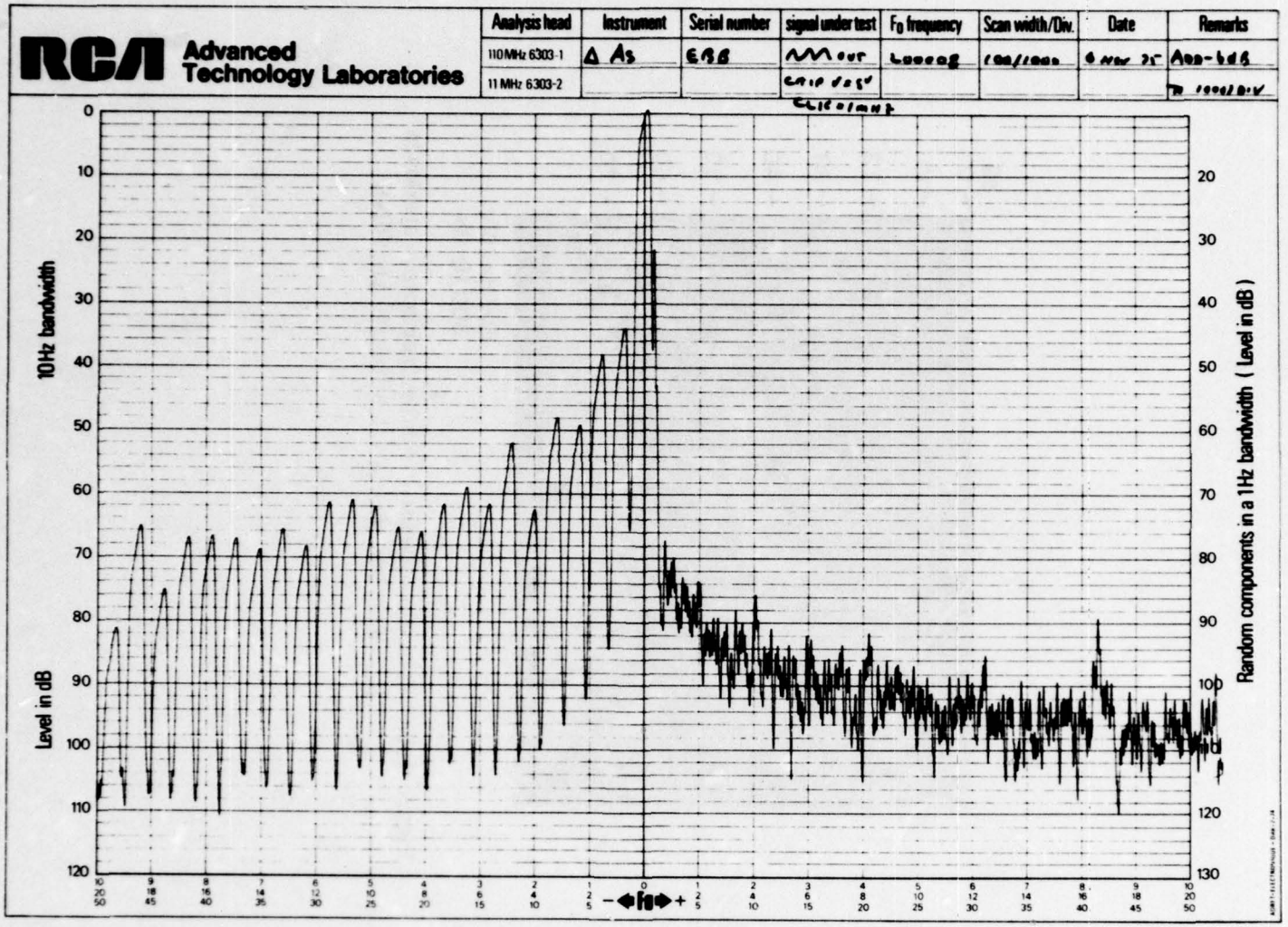


Figure 93a. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

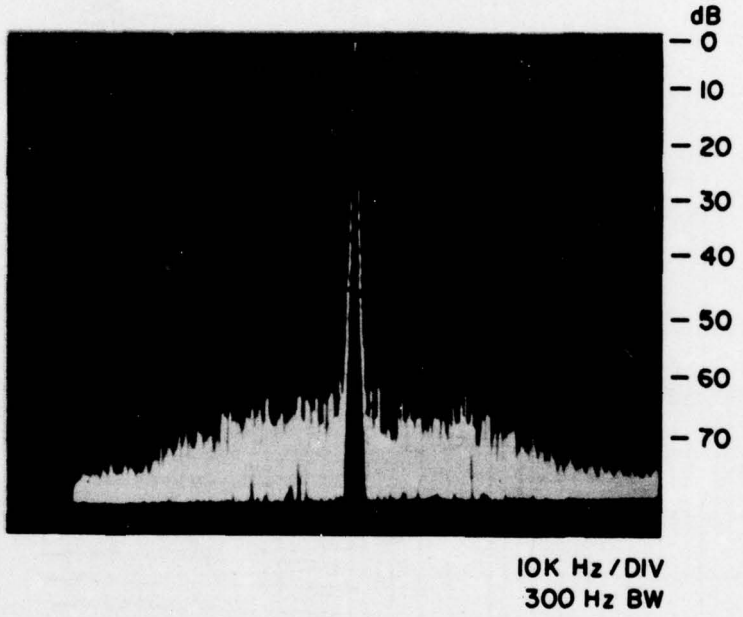


Figure 93b. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 1 MHz) (10 kHz/div).

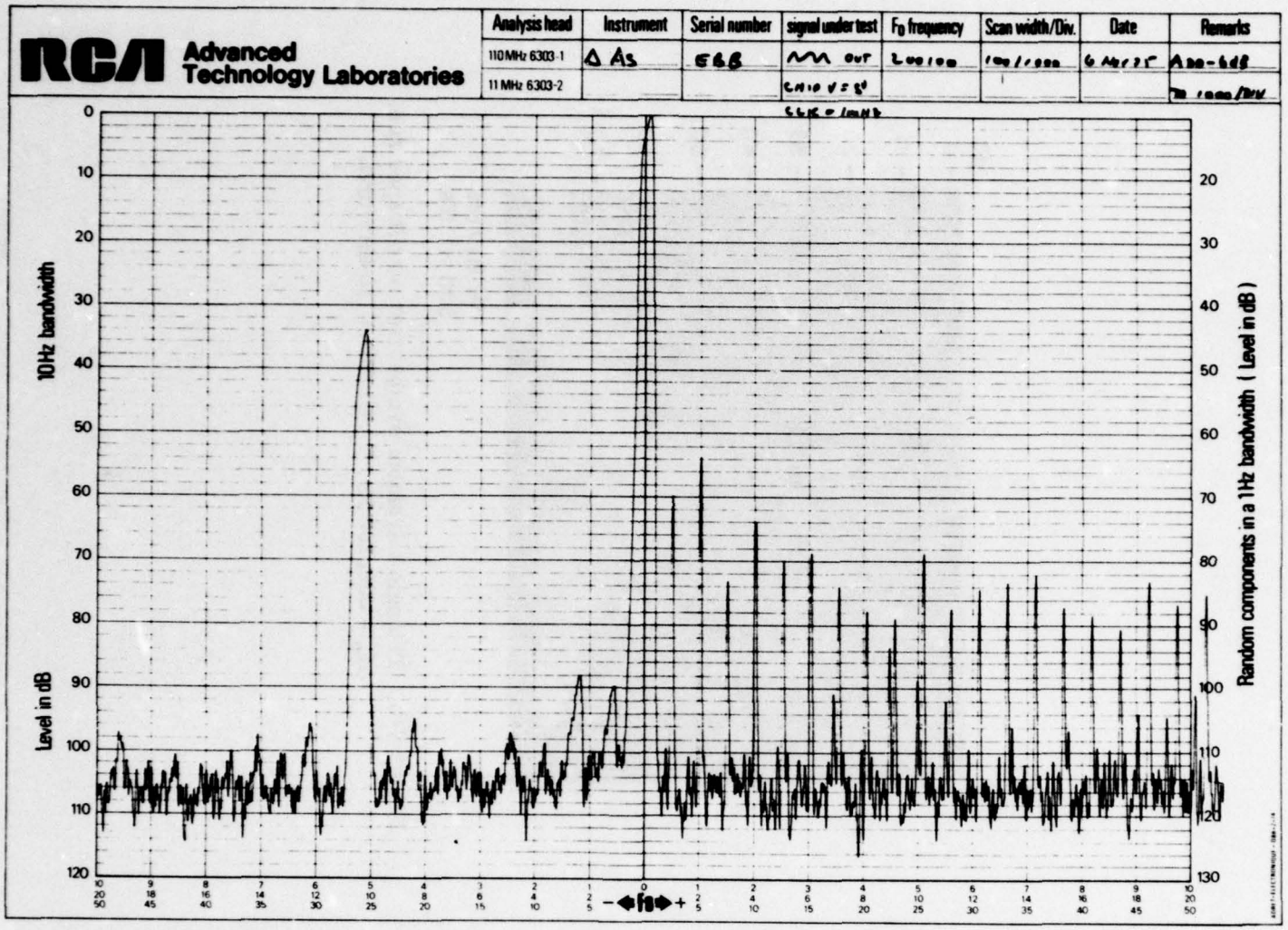


Figure 94a. Triangle waveform synthesizer output spectrum (f_o = 200,100 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

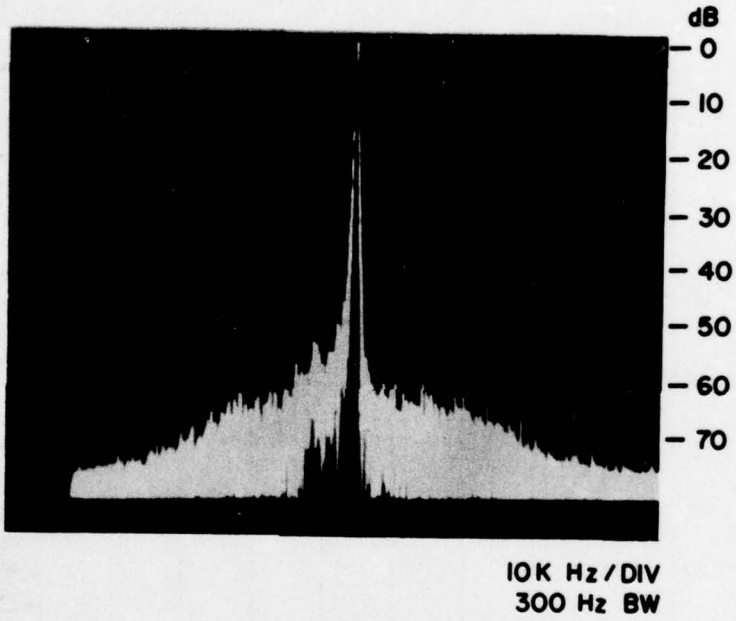


Figure 94b. Triangle waveform synthesizer output spectrum (f_o = 200, 100 Hz, f_c = 1 MHz) (10 kHz/div).

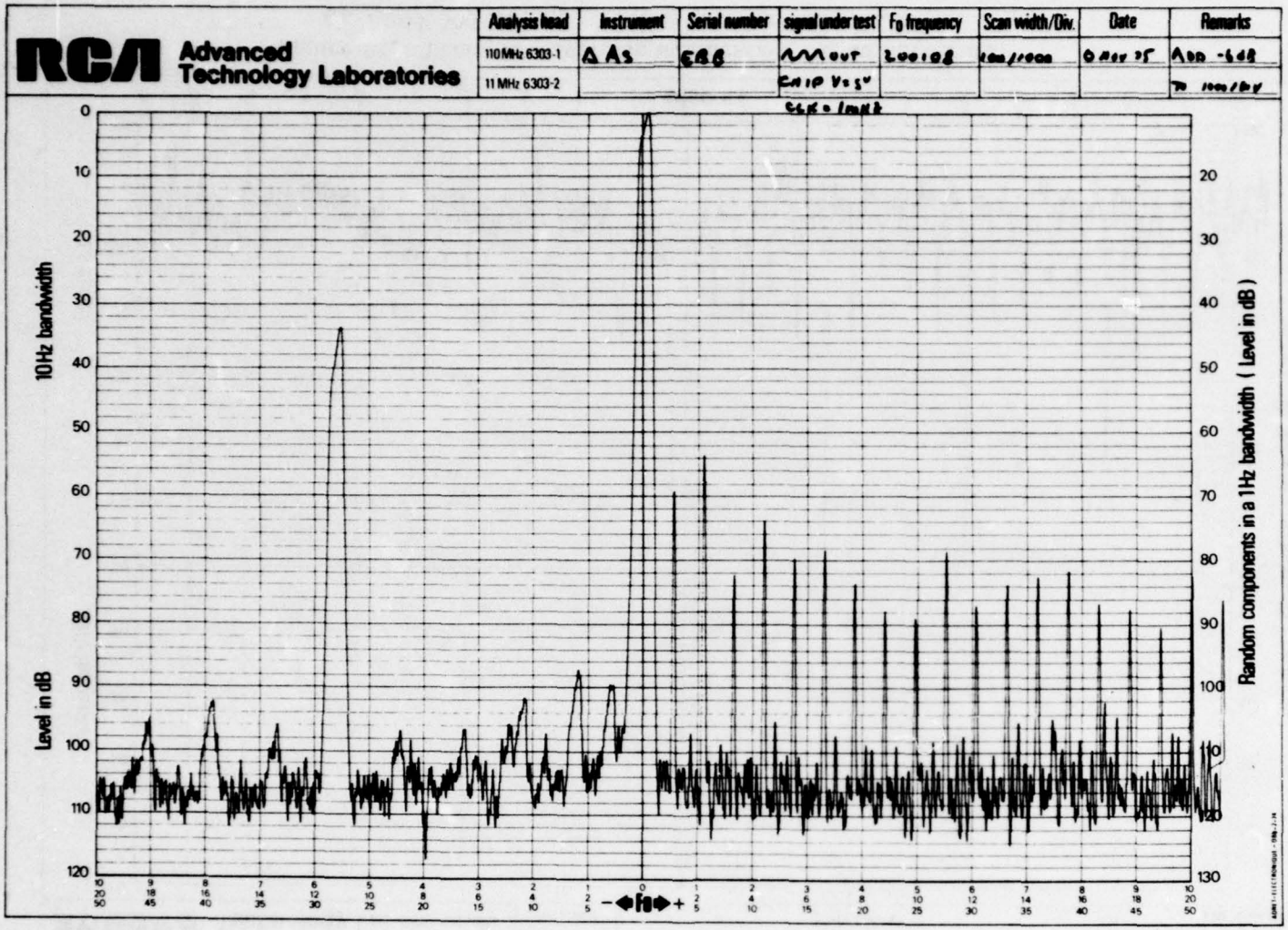


Figure 95. Triangle waveform synthesizer output spectrum (f_o = 200,108 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

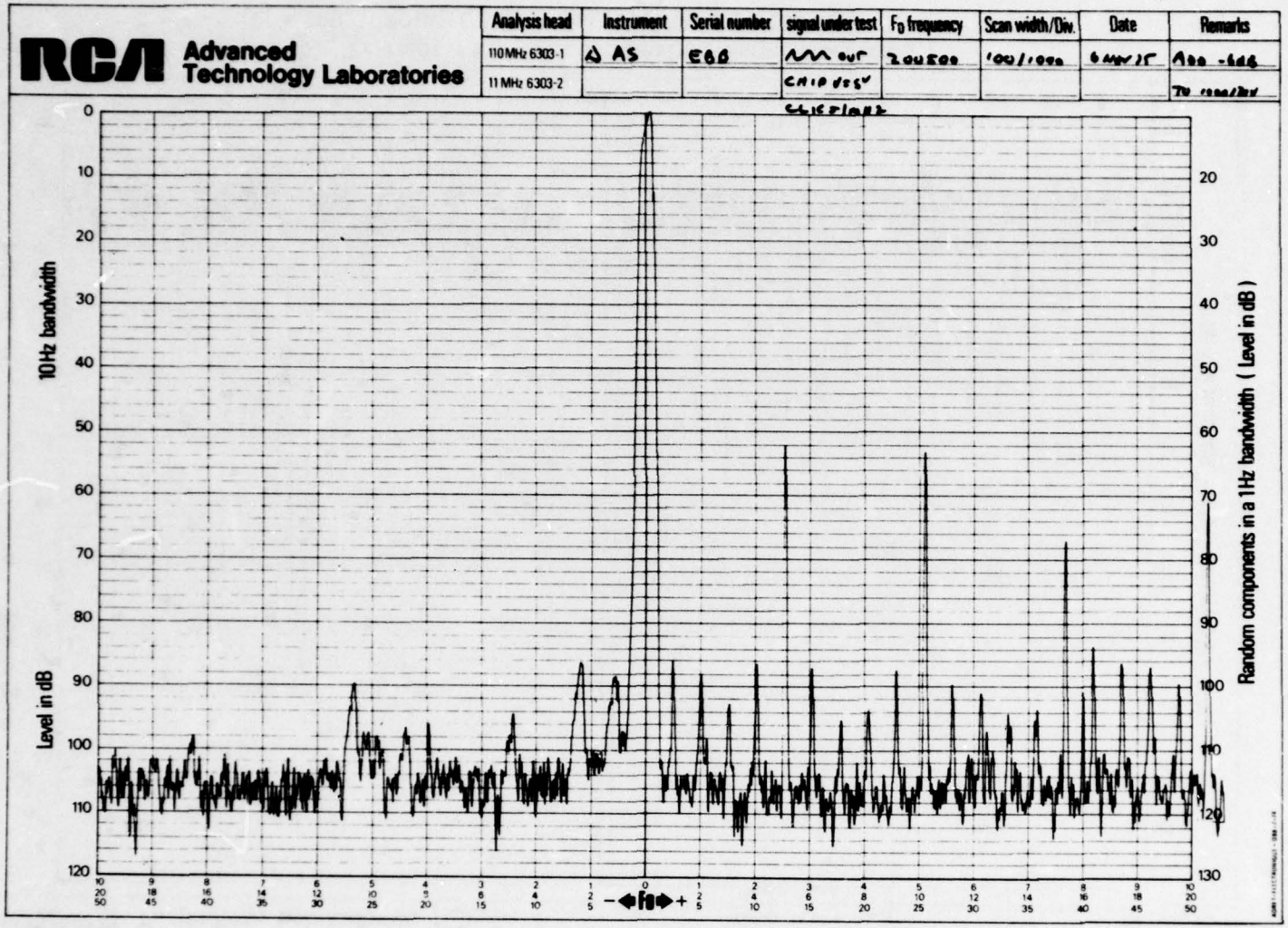


Figure 96. Triangle waveform synthesizer output spectrum (f_o = 200,500 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

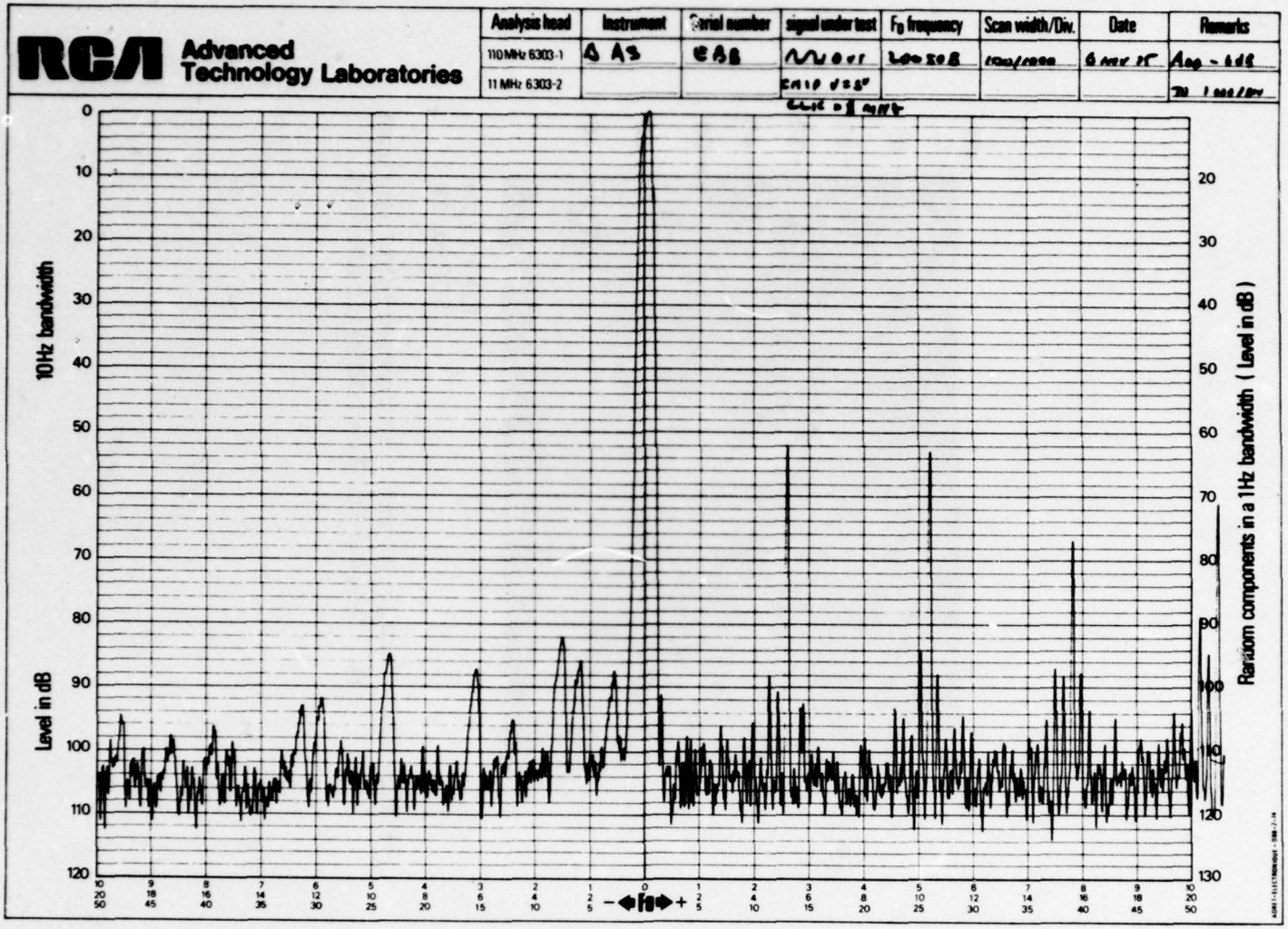


Figure 97a. Triangle waveform synthesizer output spectrum (f_o = 200,508 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

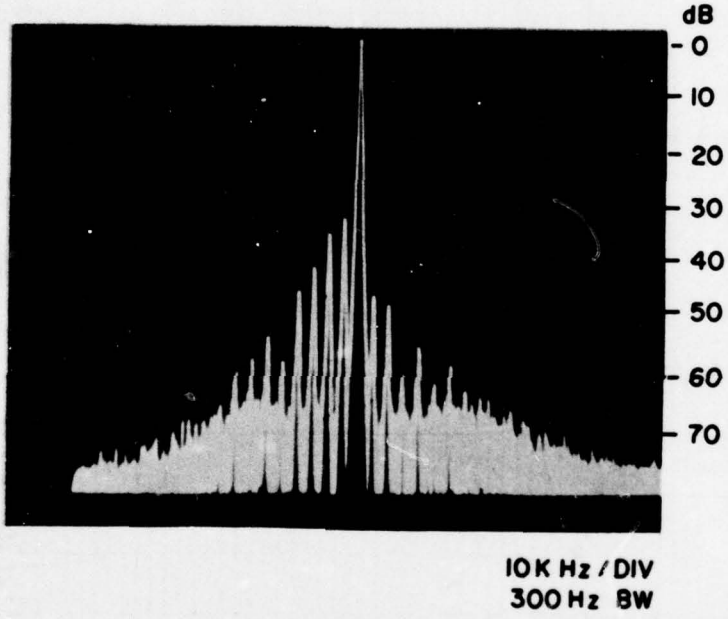


Figure 97b. Triangle waveform synthesizer output spectrum (f_o = 200, 508 Hz, f_c = 1 MHz) (10 kHz/div).

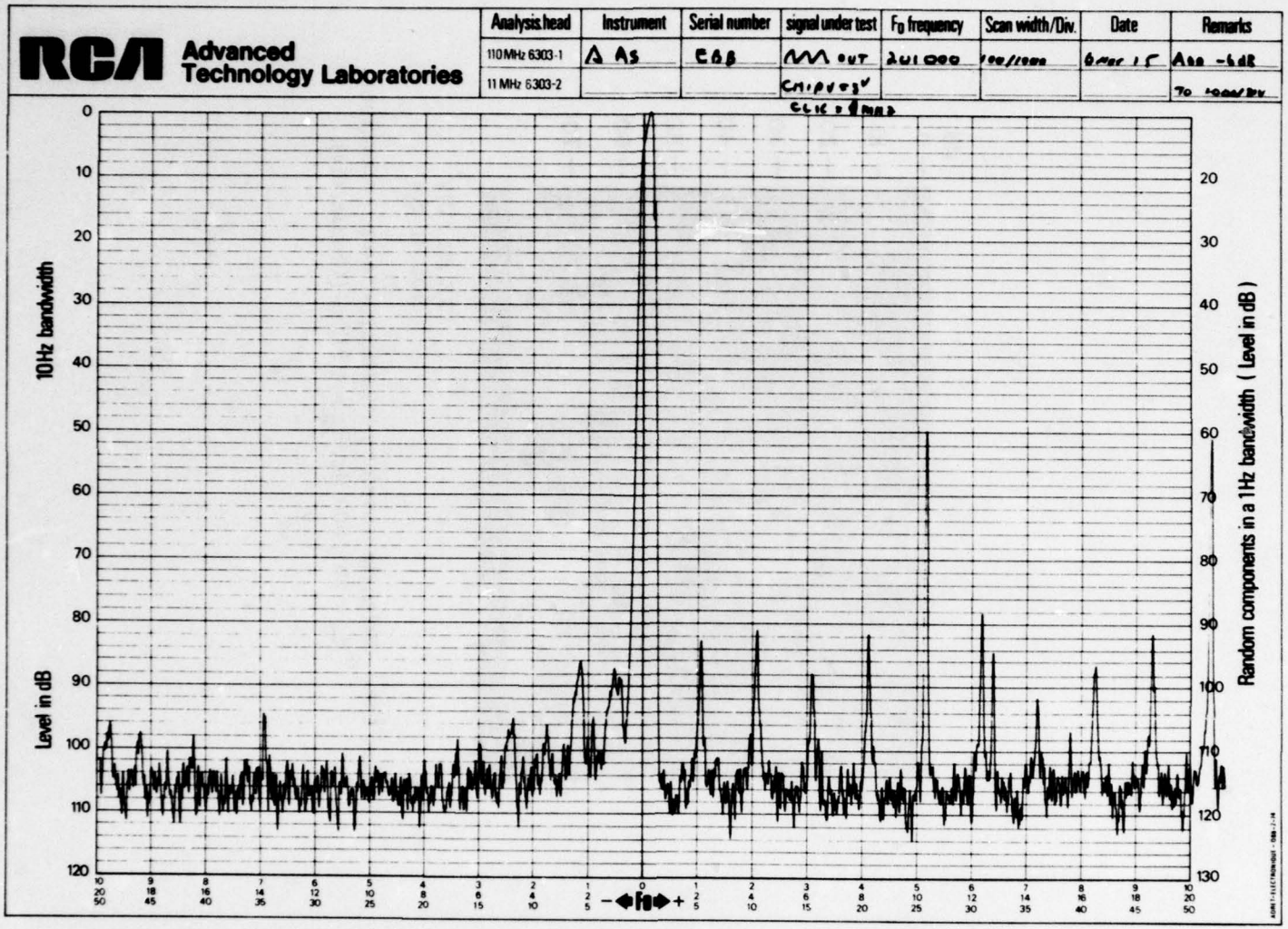


Figure 98a. Triangle waveform synthesizer output spectrum (f_o = 201,000 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

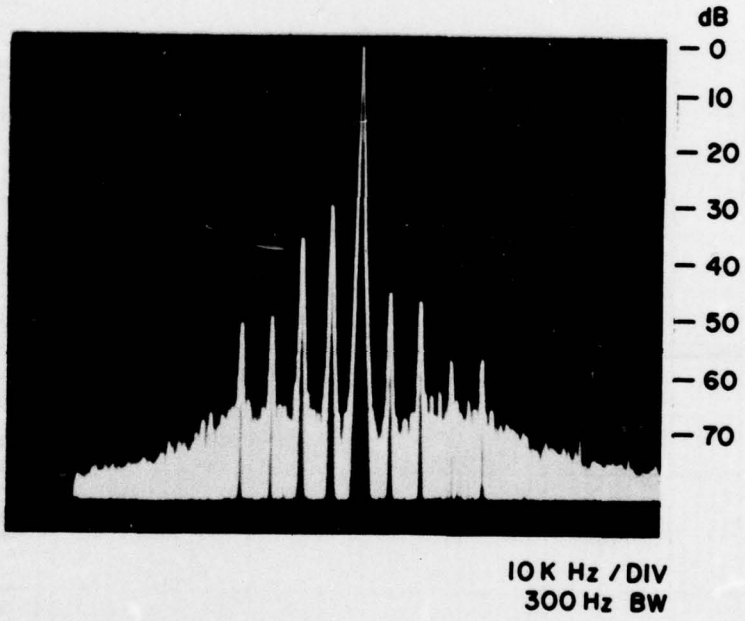


Figure 98b. Triangle waveform synthesizer output spectrum (f_o = 201,000 Hz, f_c = 1 MHz) (10 kHz/div).

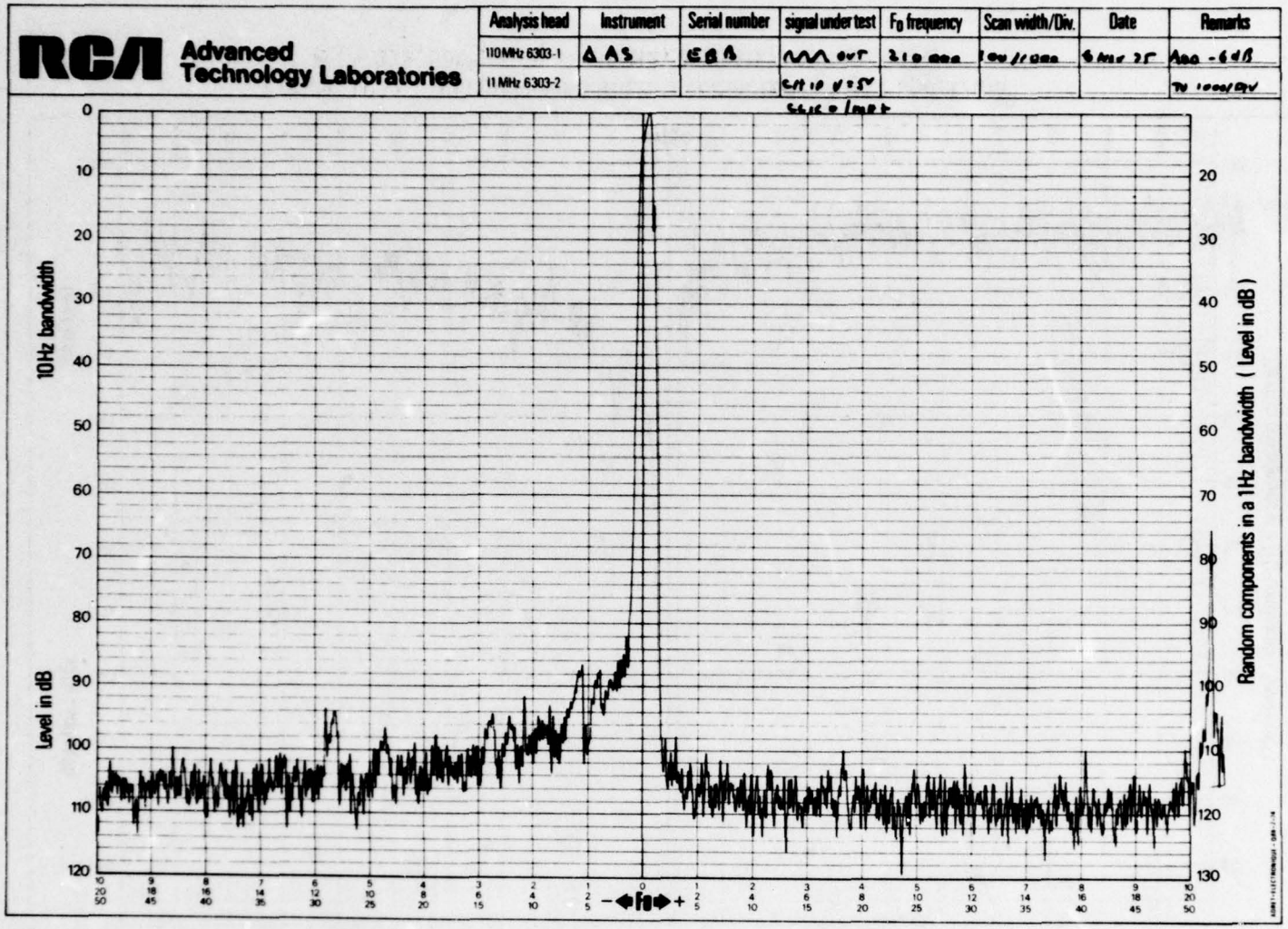


Figure 99. Triangle waveform synthesizer output spectrum (f_o = 210,000 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

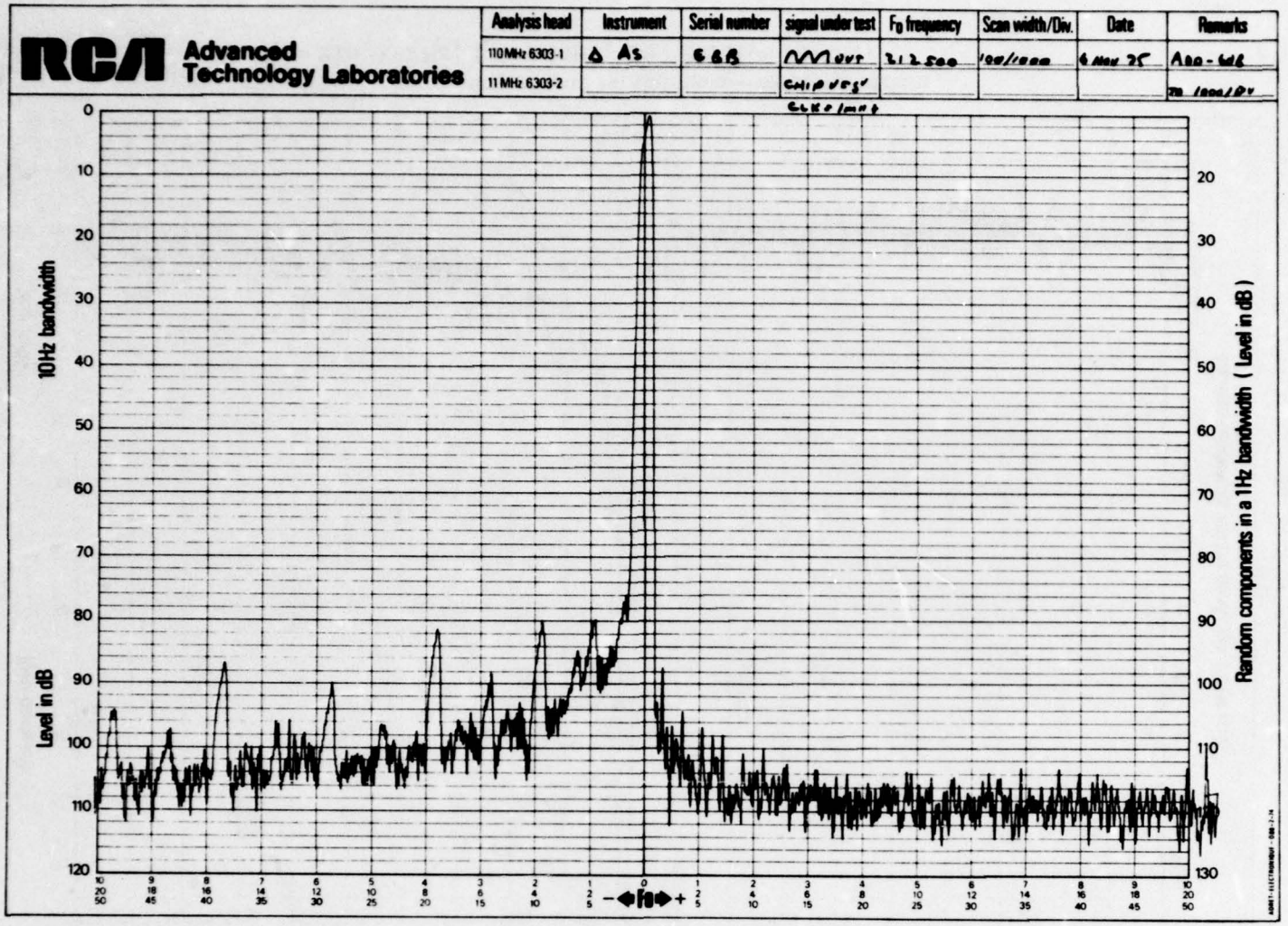


Figure 100a. Triangle waveform synthesizer output spectrum (f_o = 212,500 Hz, f_c = 1 MHz) (100 Hz/1000 Hz/div).

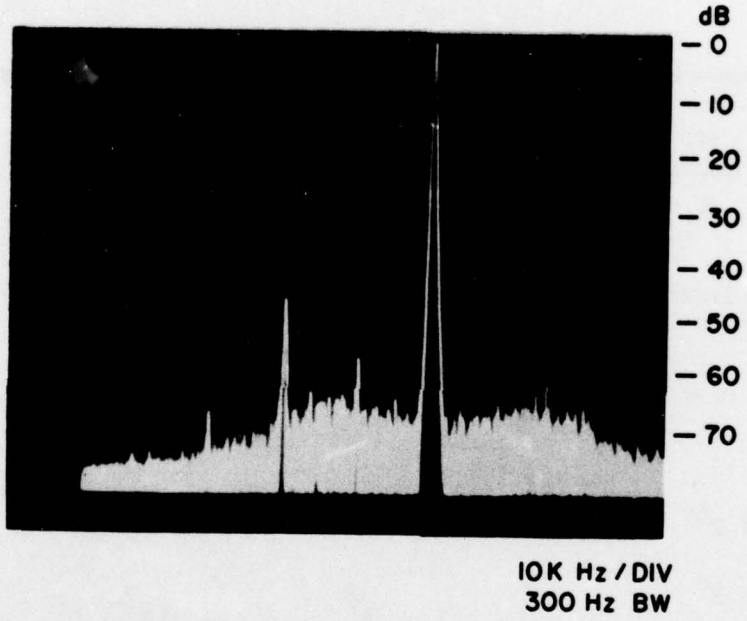


Figure 100b. Triangle waveform synthesizer output spectrum (f_o = 212,500 Hz, f_c = 1 MHz) (10 kHz/div).

Good spectral purity is a function of the ratio between synthesizer clock frequency and output frequency. A high ratio is desirable to minimize the $mf_o \pm mf_c$ product. Also, the output frequency should be an integer multiple of the ratio of the synthesizer clock to the accumulator size for good spectral purity.

On the basis of the above requirements, forcing the output band center frequency to meet the second condition above will result in a clean center frequency with spurious degradation toward the lower and upper band limit frequencies. This condition should result in the optimum combination of synthesizer clock frequency, output frequency and accumulator size for minimum spurii. Such a choice is not limited to the triangular case but also applies to the sawtooth as well.

To select the optimum clock, consider the basic AS frequency formula:

$$f_o = \frac{N_f}{N_c} f_c$$

Taking the natural logarithm of both sides and rearranging gives:

$$m = c + \frac{\ln \bar{f}_o}{\ln 2} - \frac{\ln \bar{f}_c}{\ln 2}$$

where

$N_f \equiv 2^m$

$N_c \equiv 2^c$

$\bar{f}_x = f_x$ in MHz (any frequency normalized by dividing by 10^6)

If the second term on the right is evaluated and summed with c, the following is obtained:

$$m = I.D - \frac{\ln \bar{f}_c}{\ln 2}$$

where I is the integer part and .D is the decimal part of the combination. Now, to obtain a synchronous frequency f_o:

$$I \frac{f_c}{N_c} = f_o$$

set $$\frac{\ln \overline{f_c}}{\ln 2} = .D$$

or

$$\ln \overline{f_c} = (.D) \ln 2$$

$$\overline{f_c} = \epsilon^{(.D) \ln 2}$$

$$f_c = \overline{f_c} \times 10^6$$

The f_c obtained is the "reference" f_c (= f_{cr}) and for $N_f = 2^m = 2^I$ (m = I), the output will be f_o. If f_{cr} is multiplied by 2^n (n is a ± integer), then m is decreased by n for n positive and increased by n for n negative to obtain the same output frequency.

For $N_c = 2^{24}$, f_o = 200 kHz,

$$m = 24 + (-2.32193) - \frac{\ln \overline{f_c}}{\ln 2}$$

$$= 21.67807 - \frac{\ln \overline{f_c}}{\ln 2}$$

$$\overline{f_c} = \epsilon^{(0.67807) \ln 2}$$

$$\overline{f_c} = 1.6$$

$$f_{cr} = 1.6 \text{ MHz; } m = 21.$$

For maximum spectral purity, $f_c = 2^n f_{cr}$ should be as high as possible; however, if the output bandwidth is sufficiently wide, more products of the form ($m f_o \pm f_c$) will appear in the output spectrum. For example, for f_c = 1 or 1.6 MHz, then only the product $8 f_o \pm f_c$ is troublesome. If f_c is 6.4 MHz, the products $30 f_o \pm f_c$, $31 f_o \pm f_c$, $32 f_o \pm f_c$, $33 f_o \pm f_c$ and $34 f_o \pm f_c$ can appear in the output spectrum. However, the amplitudes of these spurii will be lower by at least 10 dB. Thus, the choice of f_c becomes a compromise between number of spurii vs. amplitude and phase noise (higher f_c should have lower phase noise. These conditions can be seen in Figure 101 (1.6 MHz clock, 120 dB nominal phase noise and 30 to 70 dB spurii), Figure 102 (2 x 1.6 = 3.2 MHz clock, 126 dB nominal phase noise and 44 to 70 dB spurii), and Figure 103 (4 x 1.6 = 6.4-MHz clock, 130-dB phase noise and 54-to-70 dB spurii).

Figures 103 through 108 are for a 6.4-MHz clock. These figures show the additional in-band spurii obtained when the quantity m of the product $m f_o \pm f_c$ increases. In the case of a 1-MHz clock, high level spurii close to f_o exist only near 200 kHz. However, for a 6.4-MHz clock, high level spurii exist close to f_o at 200 kHz and 193.4 kHz (shown in Figure 106) and 206.4 kHz (shown in Figure 107). These spurii are for m = 32, 33 and 31, respectively. Other spurii exist (although no spectrum responses are shown) for m = 30 and 34; however, these will be attenuated somewhat by the output filter.

Tests of the module for f_c vs. V_{DD} for an output frequency of 200,008 Hz indicate that the maximum f_c is approximately 12 MHz at V_{DD} = 9 V. See Figures 109 through 113.

d. Settling Time Measurements

Lock-time measurements were made using the setup of Figure 114. For this test, generator f_r and the clock frequency (f_c) generator are locked to an external 1-MHz reference. Initially, f_o and f_r are offset to calibrate the scope display for a 360° peak-to-peak phase deviation. f_o is then set equal to f_r to assure a constant voltage level output on the scope from the phase detector. Frequency f_o is then offset by Δf and the scope adjusted for a single sweep triggered by the data transfer clock from the AS. Frequency f_o is then programmed to equal f_r, and the time required for the transient phase plot on the scope to reach a condition where its level deviation does not exceed ±1 vertical division (45°) of the final steady-state value is taken as the settling time to within 45° of final value, as called for in the AS/PLL specification.

Figure 115 shows settling times for the AS/PLL (staircase version) for a change from low to high, high to low, and a 1-kHz change near 200 kHz. Settling time is as follows:

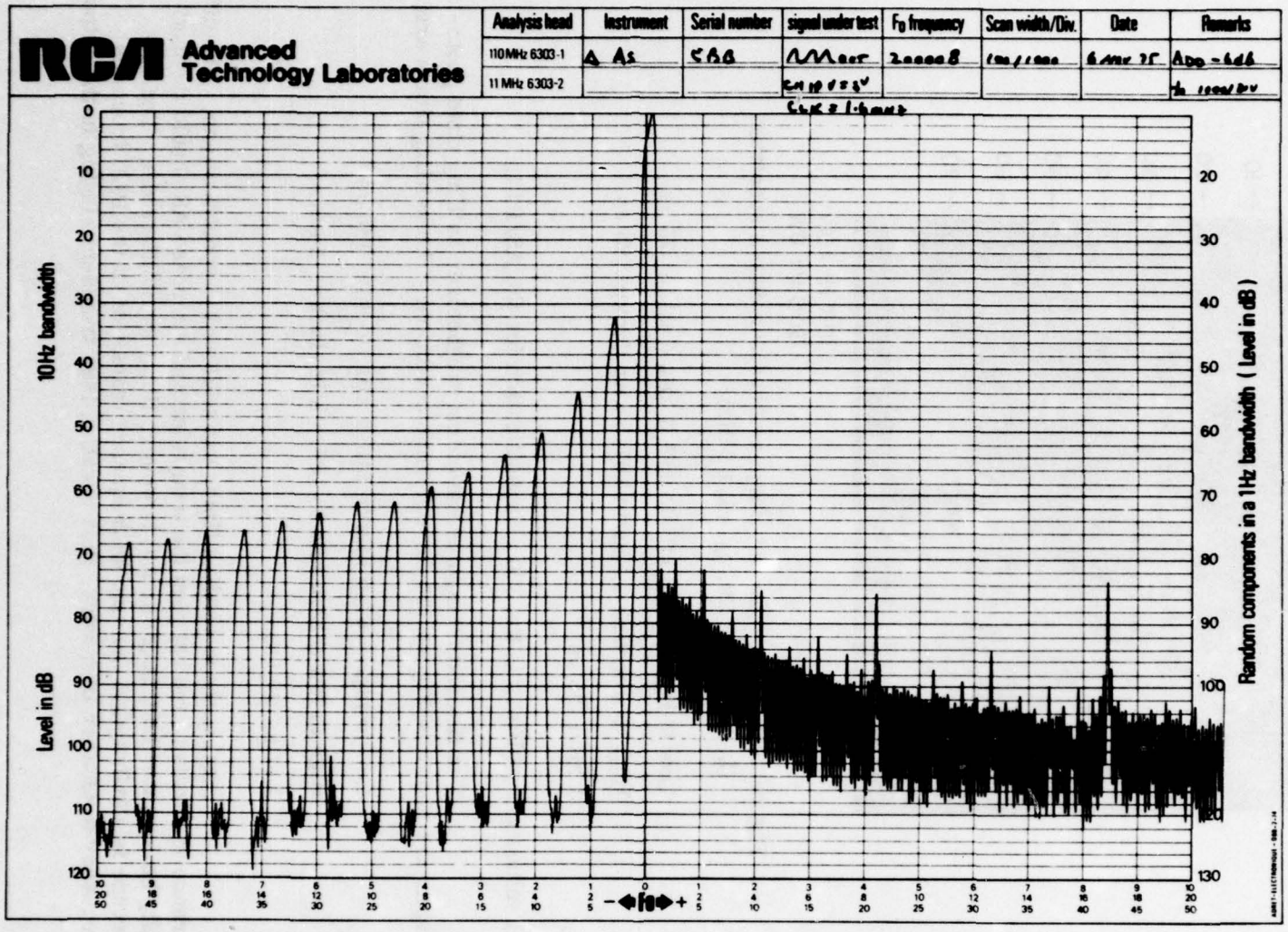


Figure 101a. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 1.6 MHz) (100 Hz/1000 Hz/div).

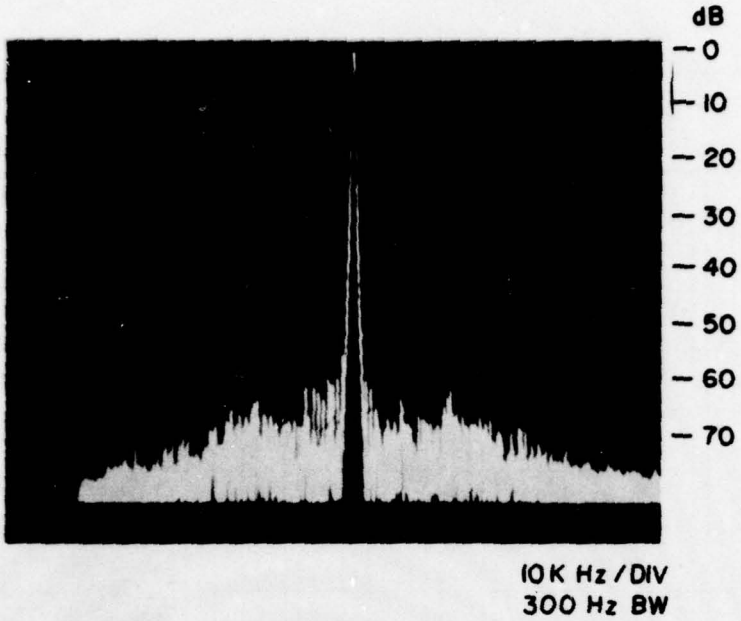


Figure 101b. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 1.6 MHz)

Low to high (187.5 kHz to 212.5 kHz (lock)): 75 μs

High to low (212.5 kHz to 187.5 kHz (lock)): 75 μs

1 kHz: 25 μs.

All values are well within the 300 μs specification for the AS/PLL.

The filtered triangular waveform synthesizer settling time photographs are shown in Figure 116 for the same condition. The settling times are:

Low to high (187.5 kHz to 212.5 kHz (lock)): 140 μs

High to low (212.5 kHz to 187.5 kHz (lock)): 140 μs

1 kHz: 25 μs.

Again, these settling times are well within specifications. The difference in settling time between the triangular and staircase AS should theoretically be less for the triangular AS; however, this was not the case. The difference is attributed to the smooth frequency transition of the PLL from one frequency to another frequency, thus creating less transient ringing in the output

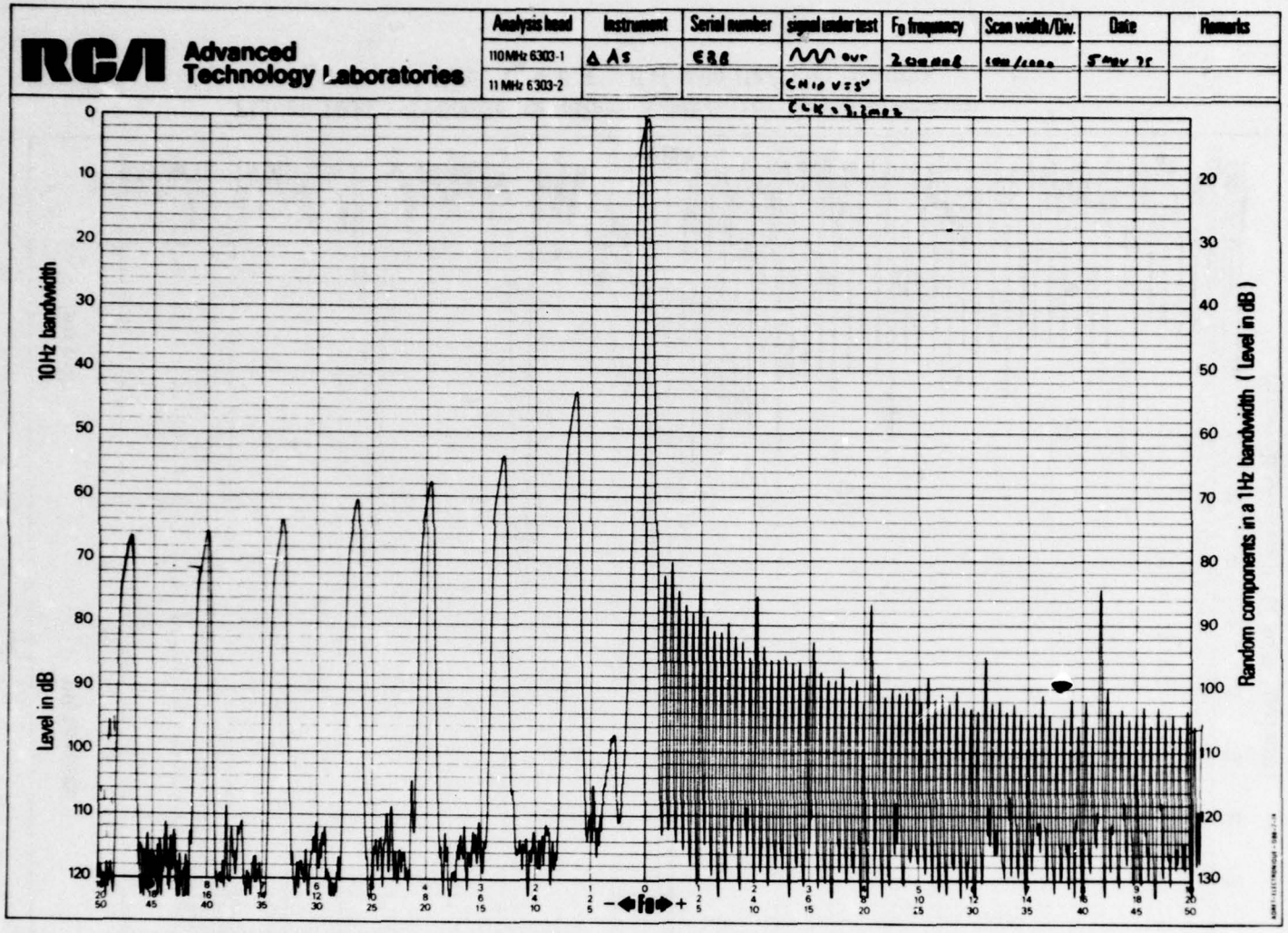


Figure 102. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 3.2 MHz) (100 Hz/1000 Hz/div).

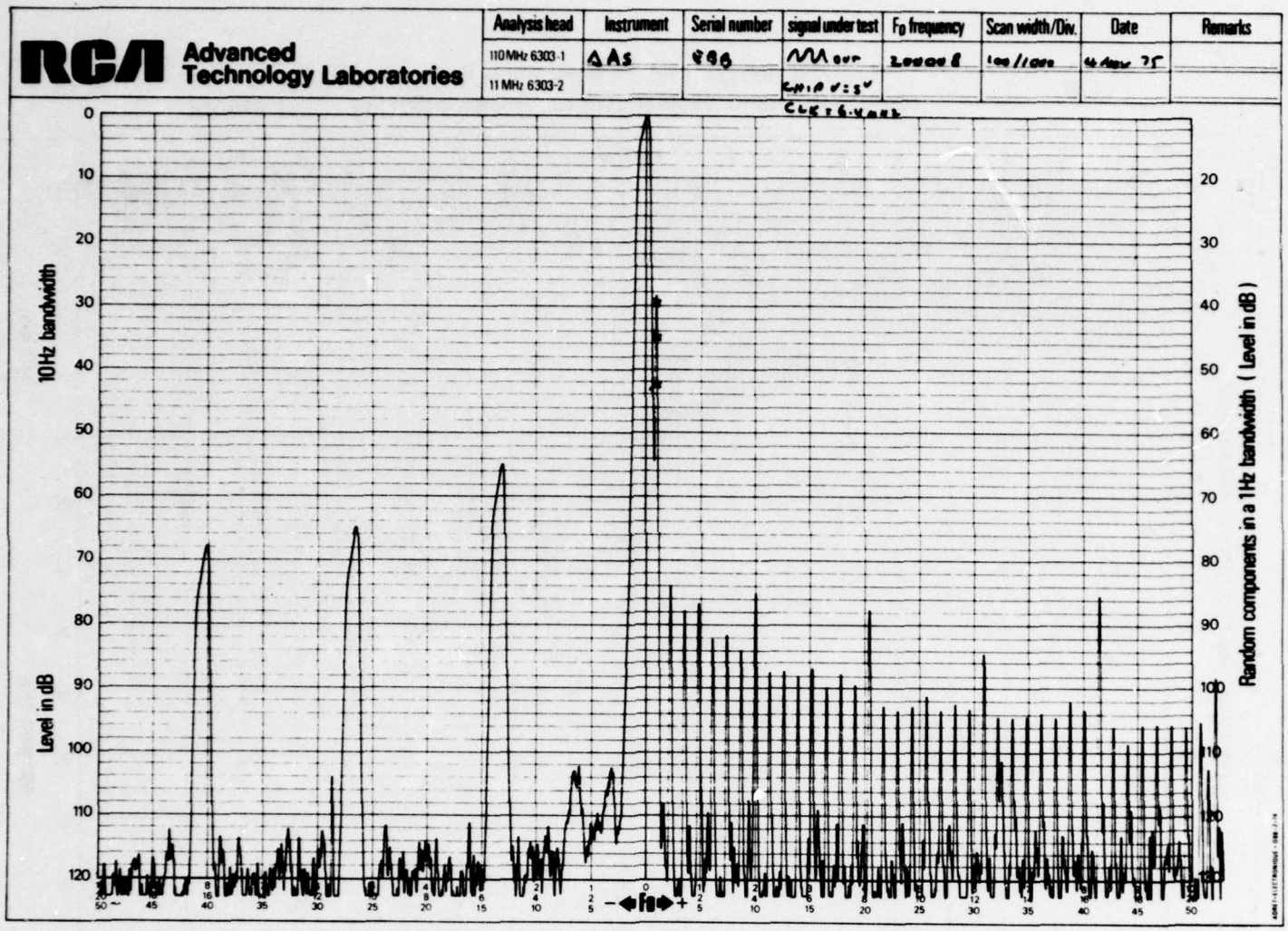


Figure 103a. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 6.4 MHz) (100 Hz/1000 Hz/div).

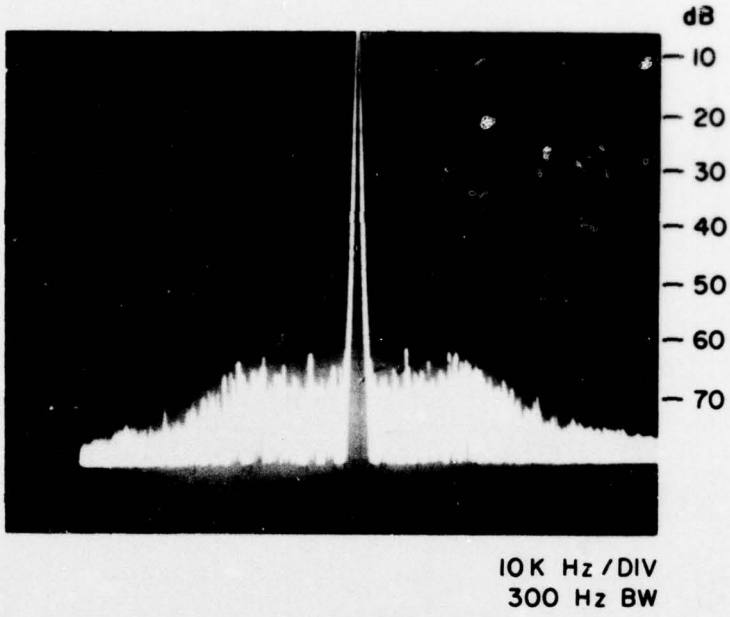


Figure 103b. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 6.4 MHz) (10 kHz/div).

filter. On the other hand, the triangular AS has a step change in frequency which should cause more ringing in the output filter and, hence, longer settling times.

e. Electrical Interface Specifications

The electrical interface specifications delineated in this section reflect the performance of the five engineering model synthesizer modules delivered under the subject contract. Although the CMOS/SOS LSI array, TCS047, that forms the basic synthesizer element, can operate over the temperature range -55° C to +125° C, the remainder of the module circuitry has not been tested over this extended temperature range.

The spectrum waveforms presented in this report have been made with the synthesizer module operating at 25° C ±10° C.

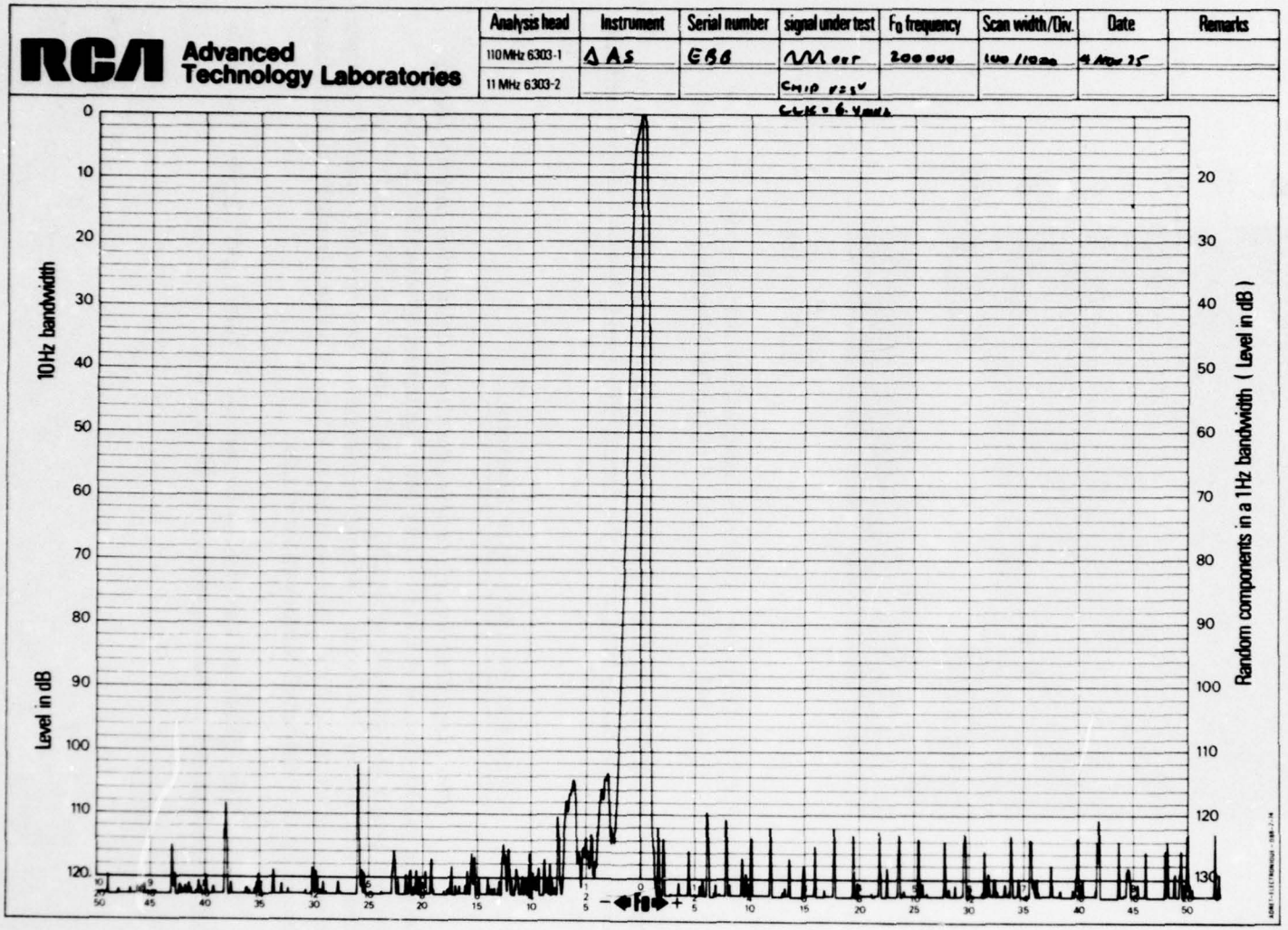


Figure 104. Triangle waveform synthesizer output spectrum (f_o = 200,000 Hz, f_c = 6.4 MHz) (100 Hz/1000 Hz/div).

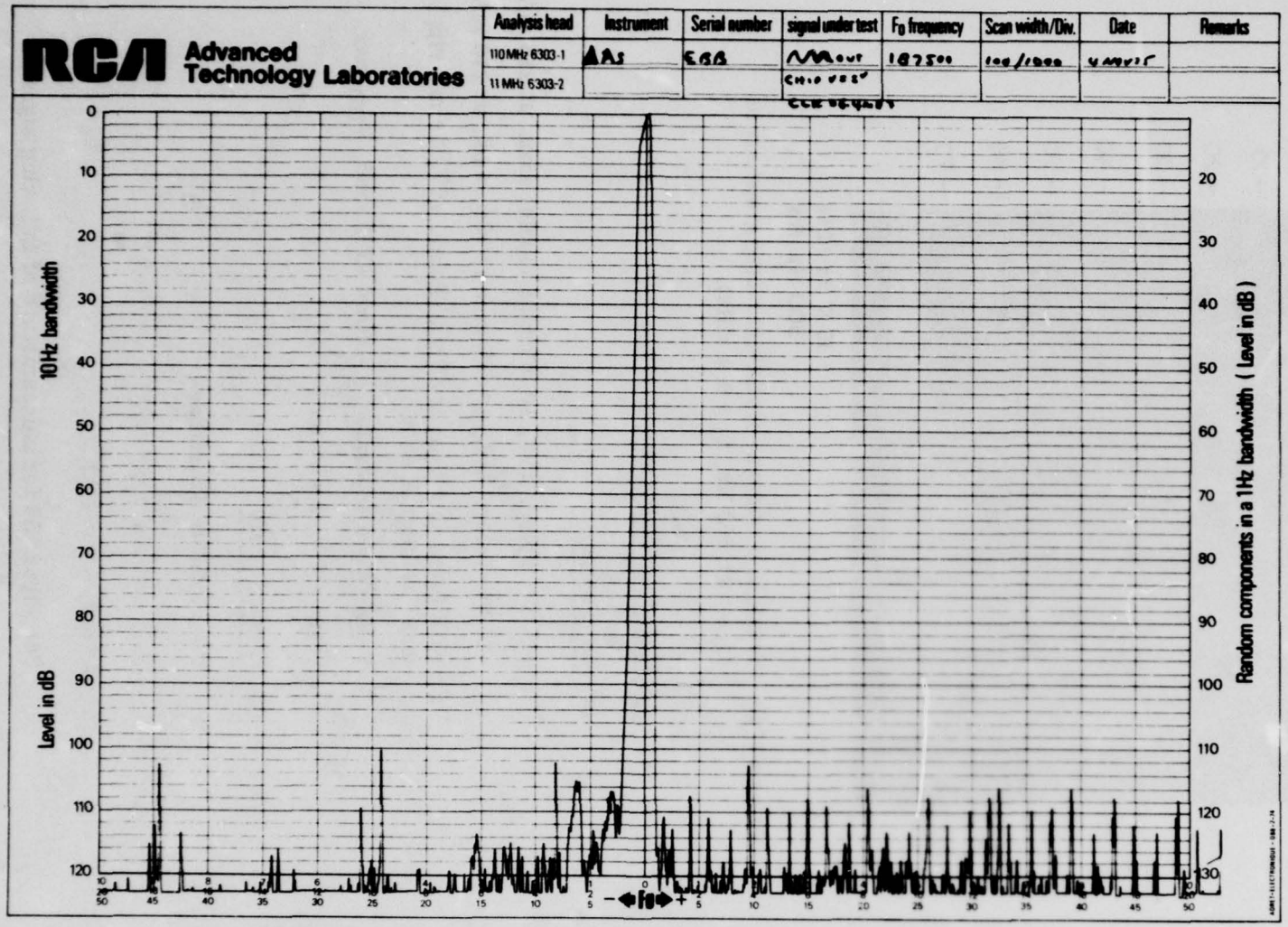


Figure 105a. Triangle waveform synthesizer output spectrum (f_o = 187,500 Hz, f_c = 6.4 MHz) (100 Hz/1000 Hz/div).

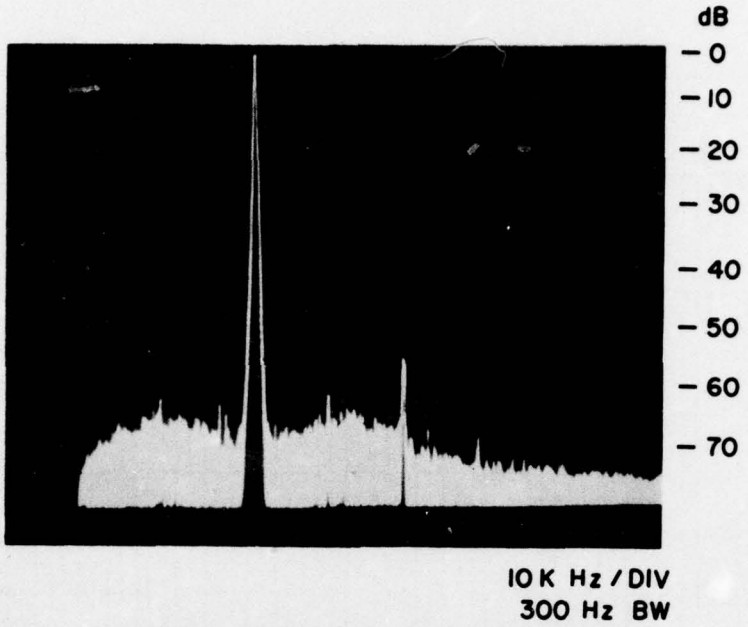


Figure 105b. Triangle waveform synthesizer output spectrum (f_o = 187,500 Hz, f_c = 6.4 MHz).

1) AS/PLL Specifications

(a) DC Power

+15 V: Toler. ±5%, 10 mV rms ripple, max. at 215 mA nom.

-15 V: Toler. ±5%, 10 mV rms ripple, max. at 215 mA nom.

+5 V (including V_{DD} at +5 V): Toler. ±5%, 10 mV ripple, max. at 290 mA nom.

V_{DD}: When separate V_{DD} from +5 V used, V_{DD} max. = 12 V. (V_{DD} = 5 V, I = 15 mA)

(b) Clock Signals

TTL level is defined as:

0 = 0 < V < 0.7 V

1 = 2.4 < V < 5 V

See Figure 55 for nomenclature of following signals:

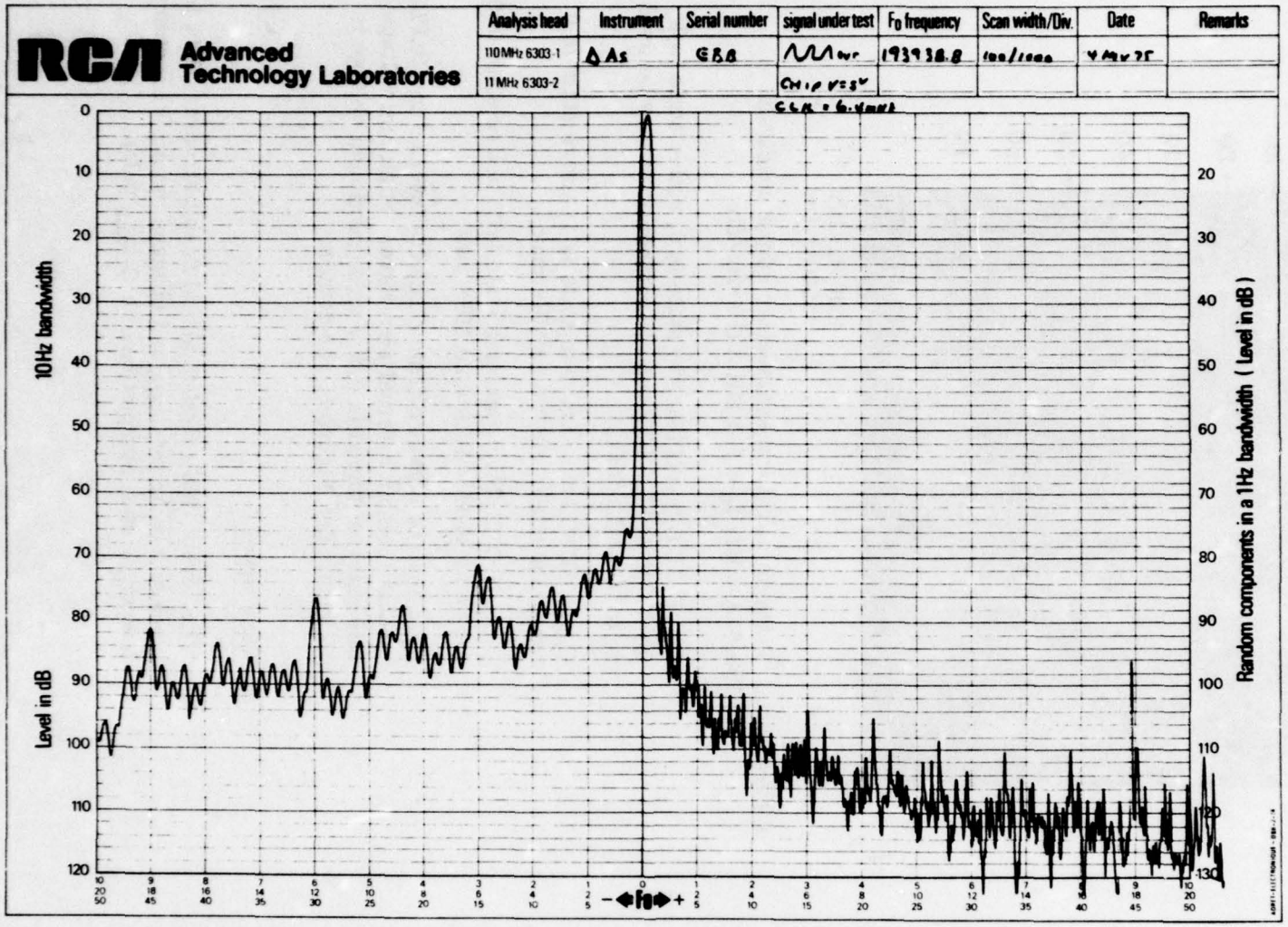


Figure 106a. Triangle waveform synthesizer output spectrum (f_o = 193,938.8 Hz, f_c = 6.4 MHz)(100 Hz/1000 Hz/div).

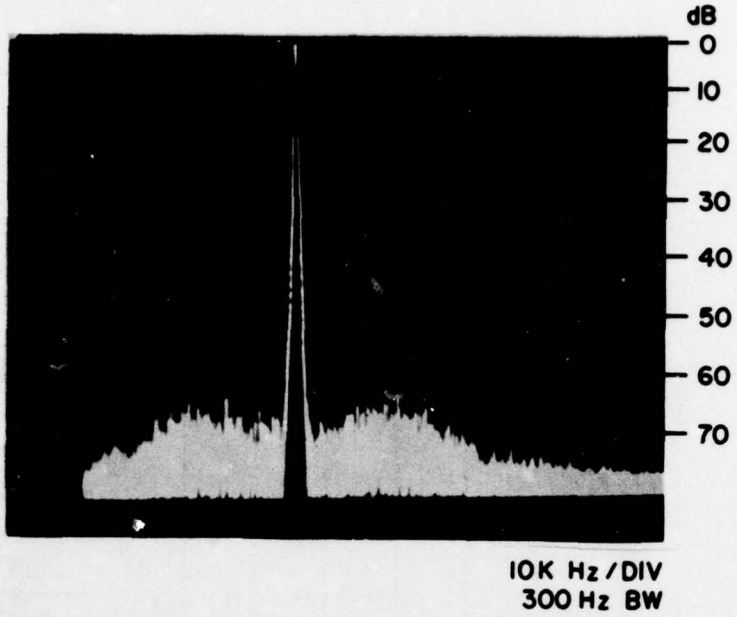


Figure 106b. Triangle waveform synthesizer output spectrum (f_o = 193,938.8 Hz, f_c = 6.4 MHz) (10 kHz/div).

C_{syn}: TTL level; inactive state is 0; active state is 1 for 75 ns ±10%. PRR = 1 MHz (other PRR may be used up to 3.5 MHz max.)

C_{data}: TTL level; inactive state is 1; active state is 0 for 25 ns ±10%. PRR = 20 MHz max.

C_{trans}: TTL level; inactive state is 1; active state is 0 for 75 ns ±10%. PRR = 20 MHz max.

C_{syn} may be obtained from circuitry internal to AS/PLL module from an external sine wave. Minimum voltage of this external signal is 0.2 V rms; maximum voltage is 1V rms. See Figure 55 for details.

(c) Data Signal

TTL levels, MSB first in serial 24-bit stream. Data is clocked into AS by C_{data} and changes the AS/PLL output frequency upon completion of a C_{trans} pulse.

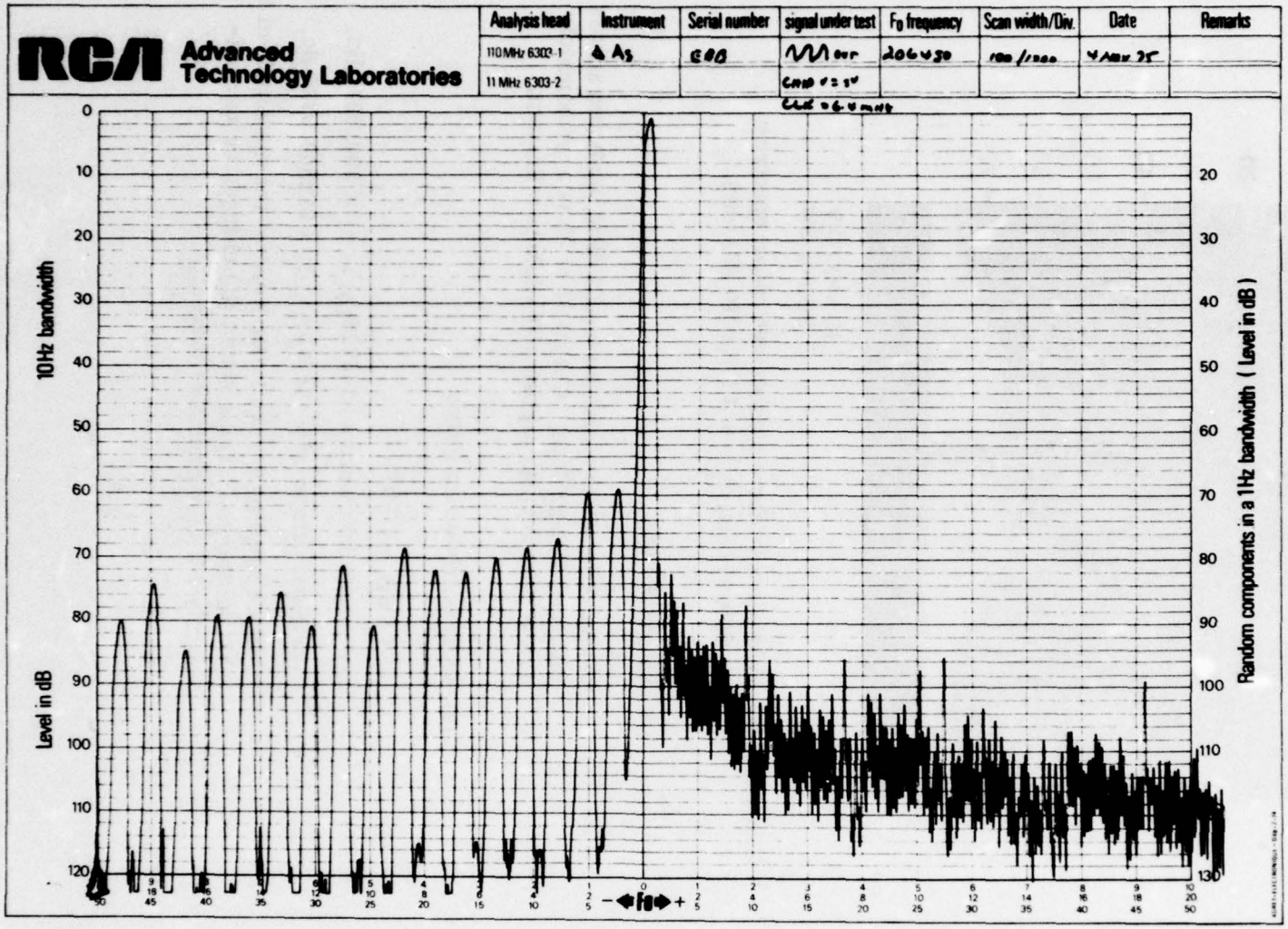


Figure 107a. Triangle waveform synthesizer output spectrum (f_o = 206,450 Hz, f_c = 6.4 MHz)(100 Hz/1000 Hz/div).

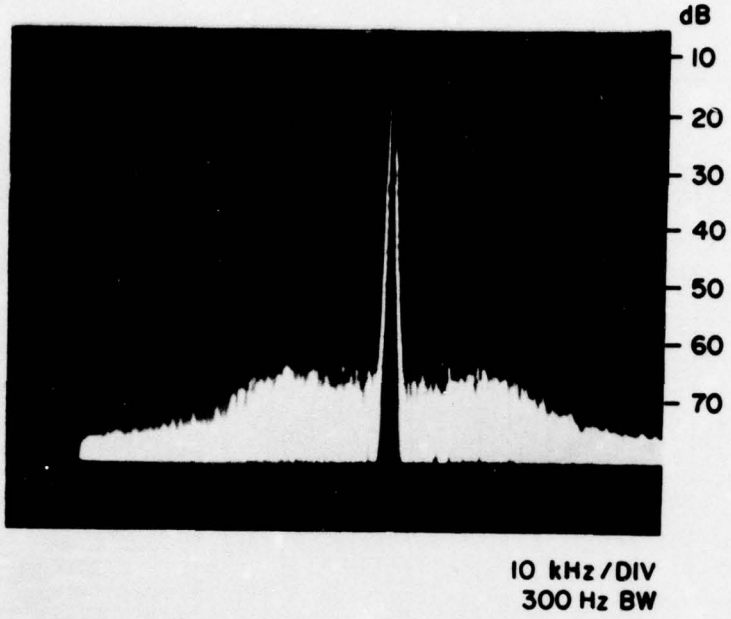


Figure 107b. Triangle waveform synthesizer output spectrum (f_o = 206,450 Hz, f_c = 6.4 MHz)(10 kHz/div).

(d) Output Signals

Output #1 at J1 is a sine wave at 3 dBm minimum across 50-ohm, 100-pF load. Output #2 at J2 is approximately 1.6 V p-p sawtooth across 100 kilohms minimum.

(e) Output Frequency Range

For C_{syn} = 1 MHz.

For input data word = 3145728_{10}; f_o = 187500.0007 Hz.

For input data word = 3565159_{10}; f_o = 212500.0365 Hz.

For a change in the input data word of the magnitude of 67 (or multiples of 67) the output (f_o) changes by approximately 4 Hz (or multiples thereof).

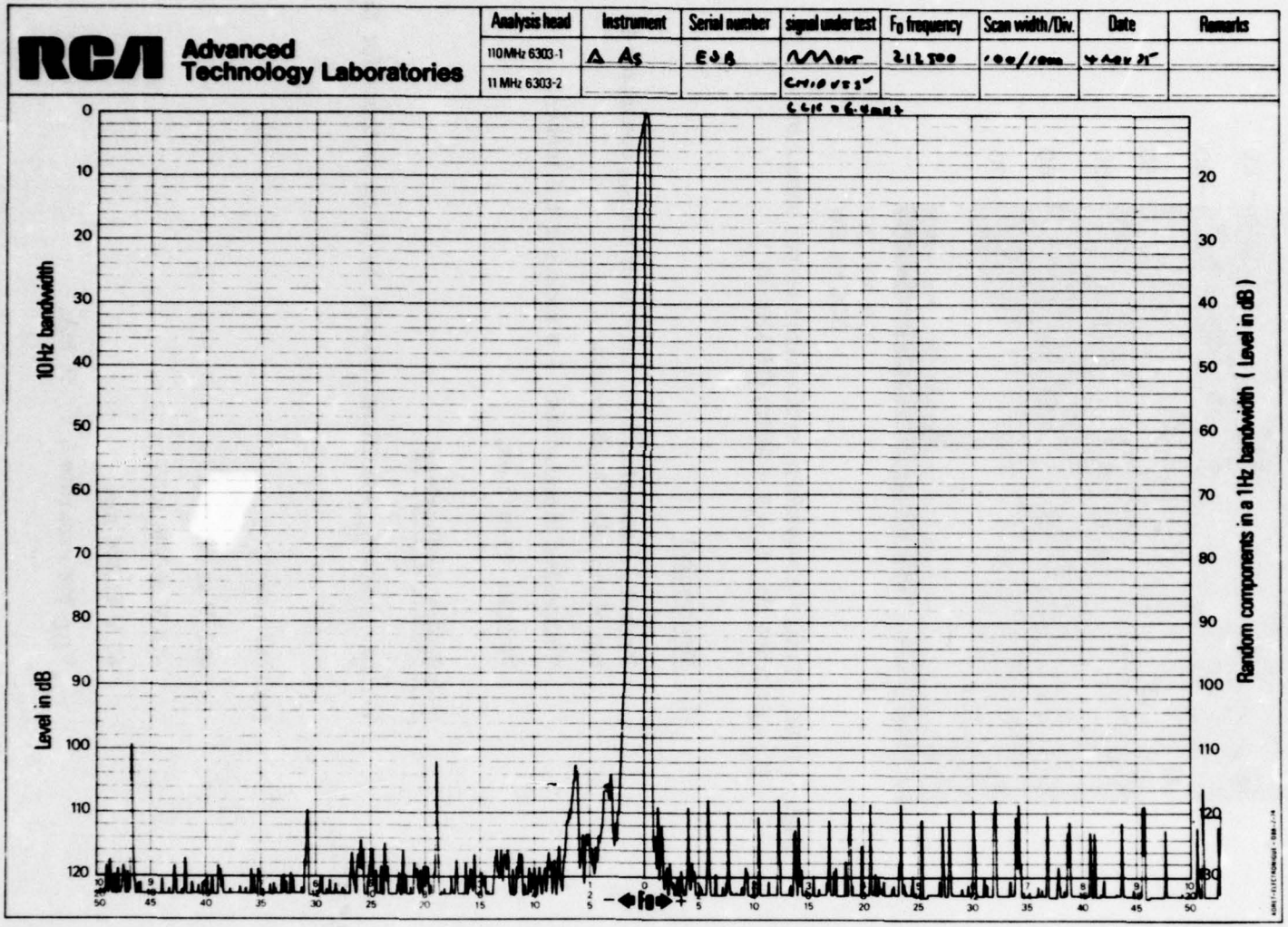


Figure 108a. Triangle waveform synthesizer output spectrum (f_o = 212,500 Hz, f_c = 6.4 MHz) (100 Hz/1000 Hz/div).

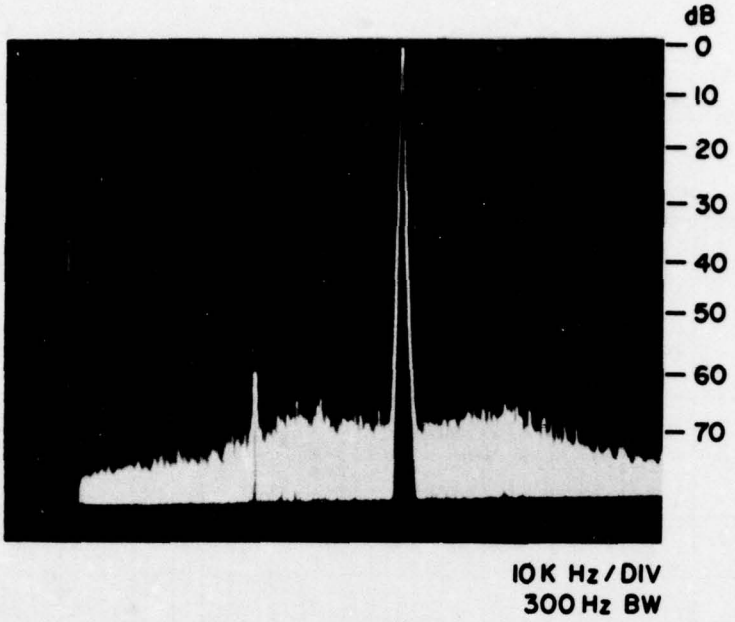


Figure 108b. Triangle waveform synthesizer output spectrum (f_o = 212,500 Hz, f_c = 6.4 MHz) (10 kHz/div).

(f) Mechanical

Mounted dimension from bottom of mating connector to top of module: 8.45 inches.

Unmounted dimensions: 8.3 inches x 4.5 inches.

Weight: 11-3/8 oz.

2) Triangular Synthesizer

Where not noted, specifications are the same as those for the AS/PLL.

(a) DC Power

+15 V at 160 mA

-15 V at 160 mA

+5 V at 250 mA

V_{DD} for separate 5 V, 36 mA.

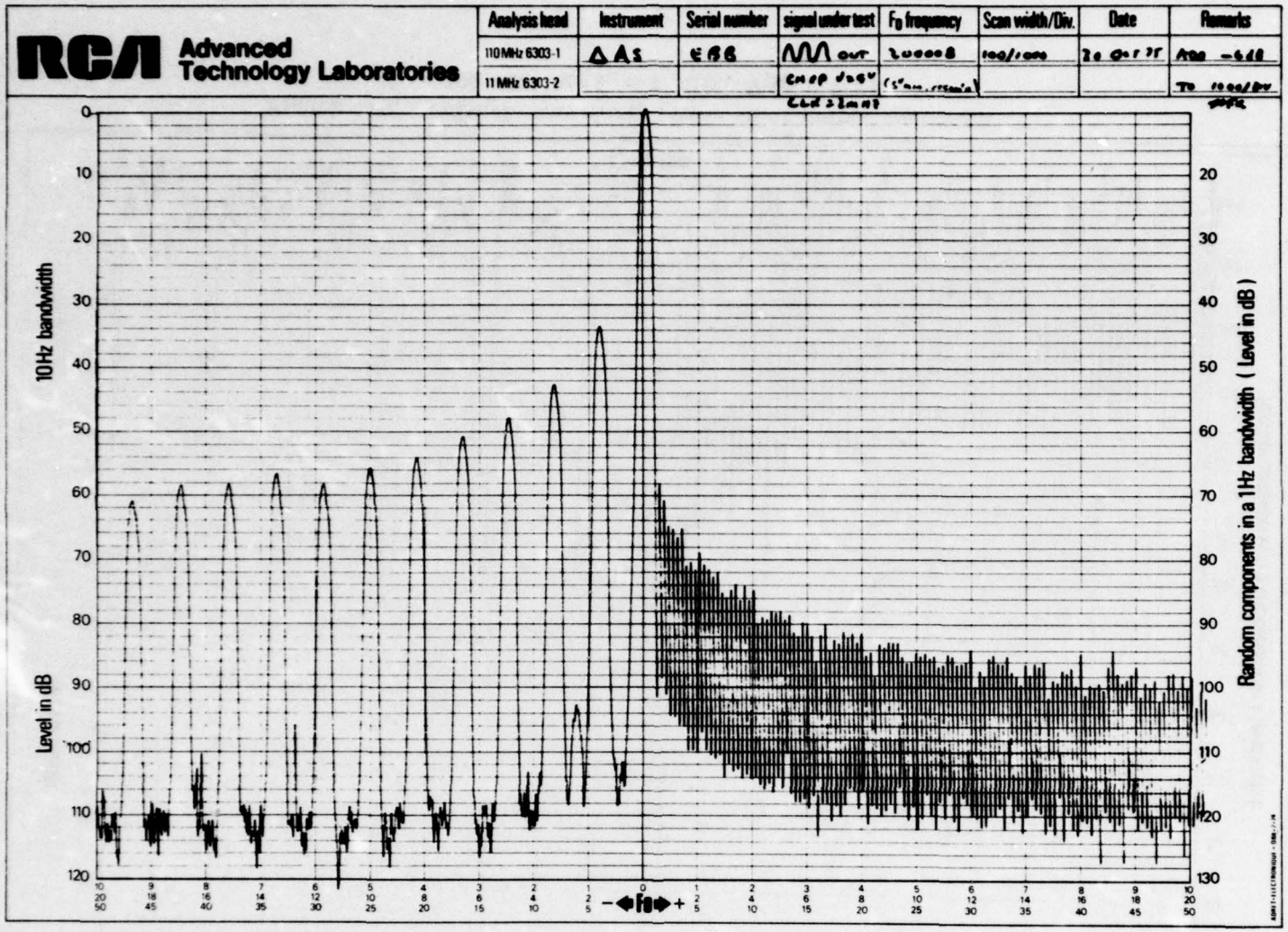


Figure 109. Triangle waveform synthesizer output spectrum (f_O = 200,008 Hz, f_C = 2 MHz, V_{DD} = 9 V).

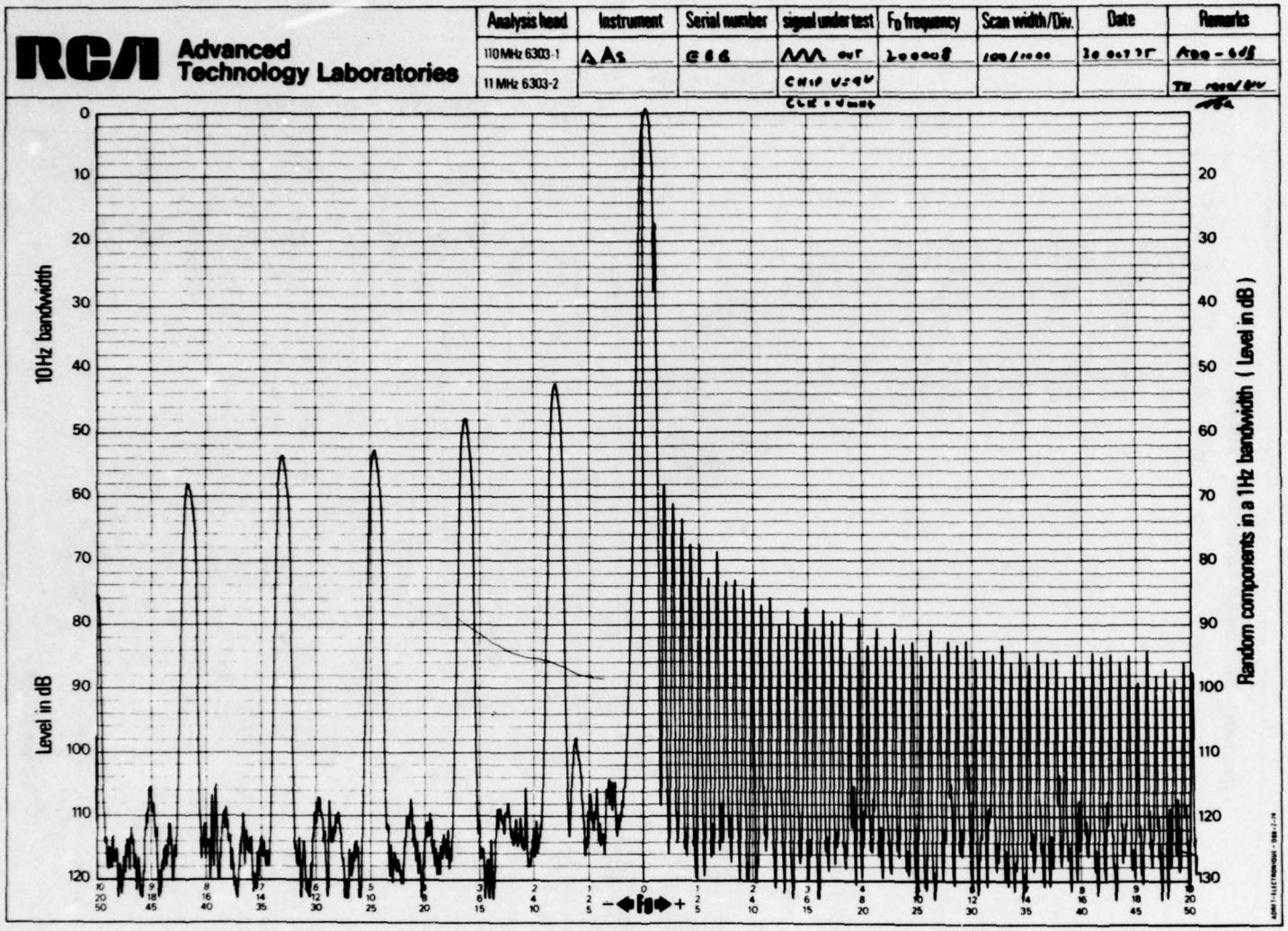


Figure 110. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 4 MHz, V_{DD} = 9 V).

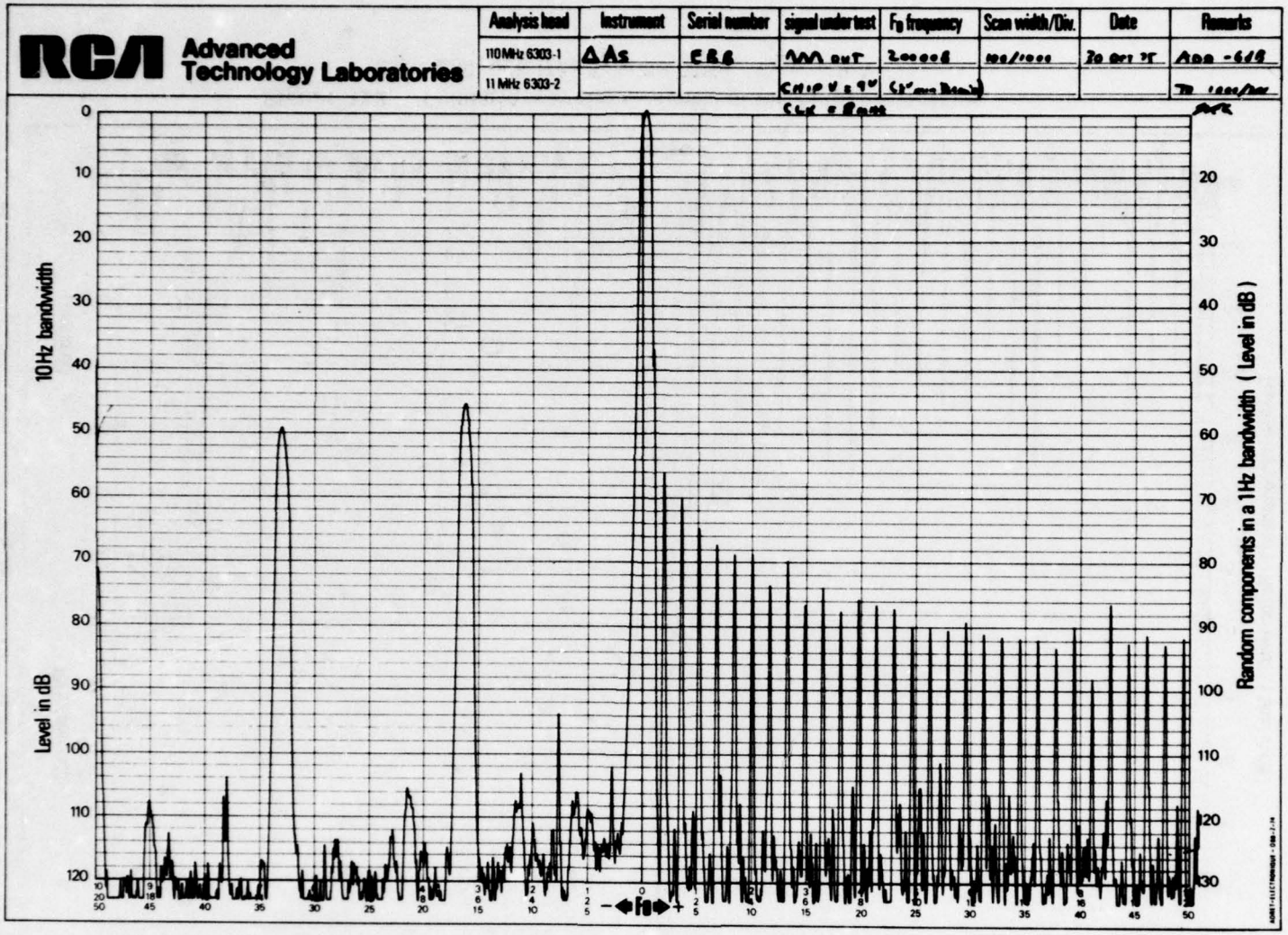


Figure 111. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 8 MHz, V_{DD} = 9 V).

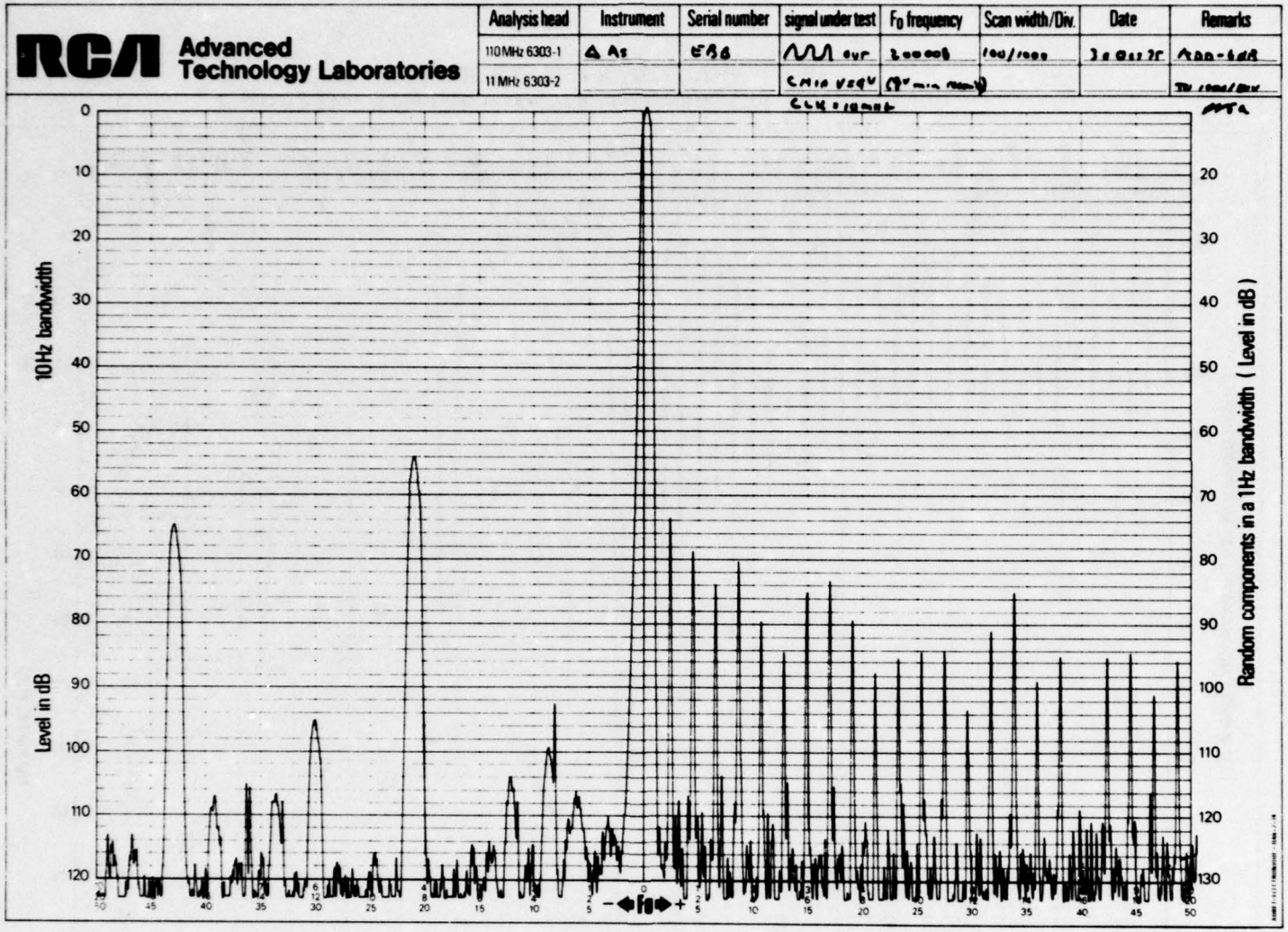


Figure 112. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 10 MHz, V_{DD} = 9 V).

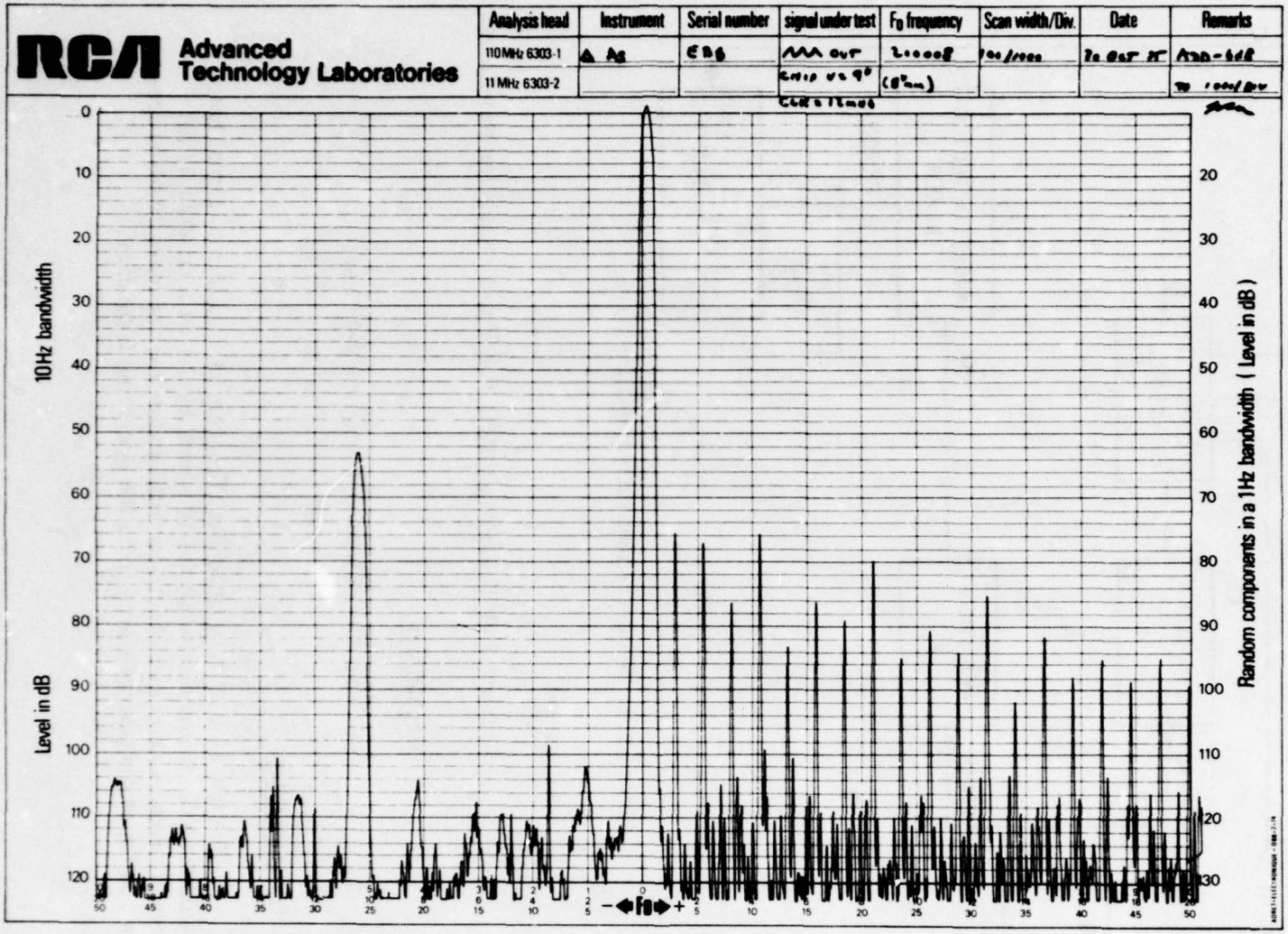


Figure 113. Triangle waveform synthesizer output spectrum (f_o = 200,008 Hz, f_c = 12 MHz, V_{DD} = 9 V).

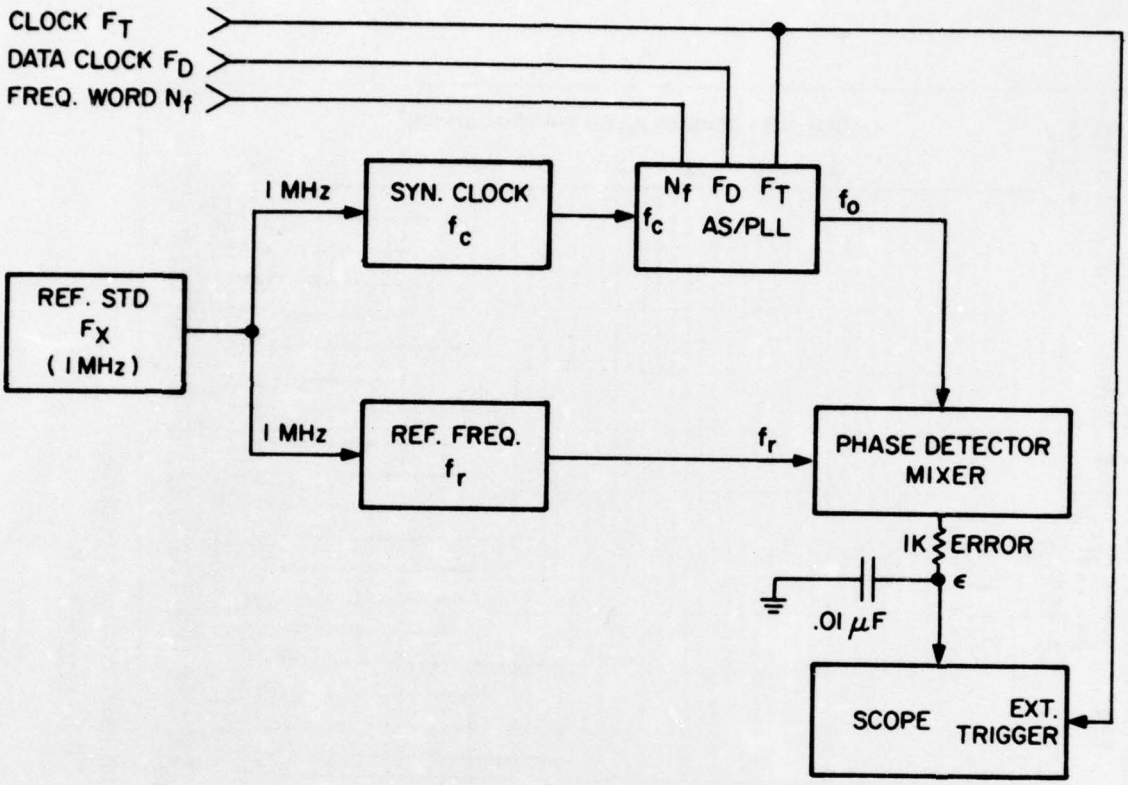


Figure 114. Setup for measuring settling time.

(b) Output

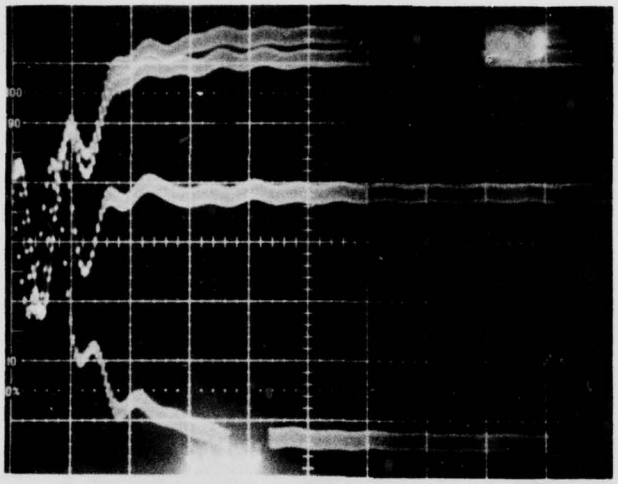
Number 2 at J2 approximately 0.8 V p-p triangular waveform.

(c) Mechanical

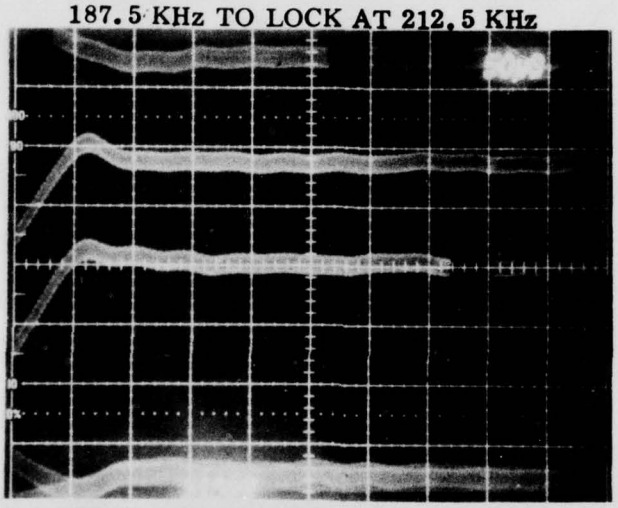
Same as AS/PLL except weight = 9-1/8 oz.

f. Summary

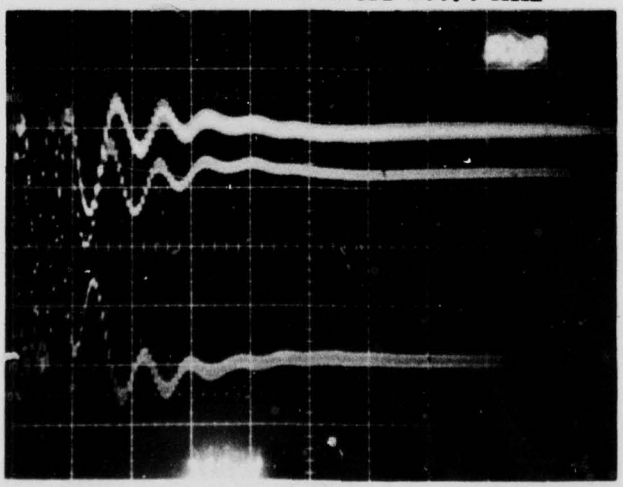
The use of a PLL to filter the spectrum of a staircase signal has been demonstrated. Nominal attenuation of spurii by the PLL is 40 to 50 dB which should produce an output spectrum with spurii down at least 70 dB at frequencies 100 Hz or greater removed from the operating frequency.



187.5 KHz TO LOCK AT 212.5 KHz

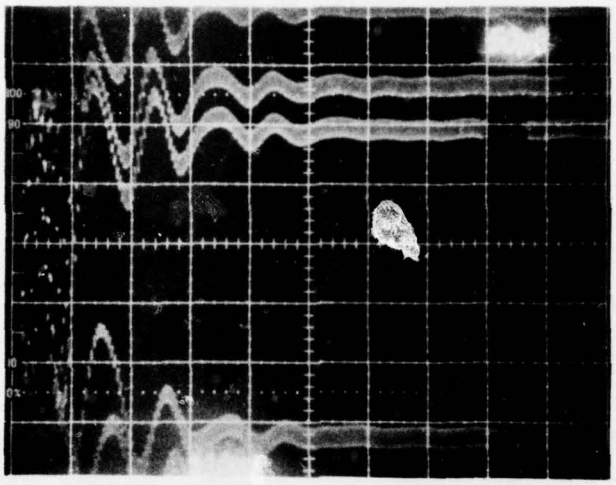


201.0 KHz TO LOCK AT 200.0 KHz

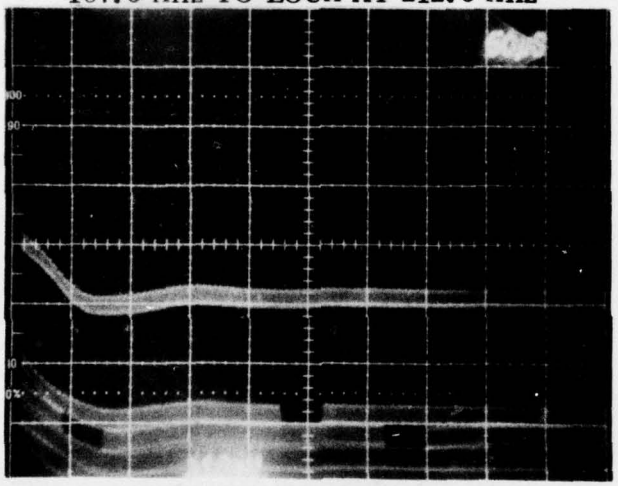


212.5 KHz TO LOCK AT 187.5 KHz

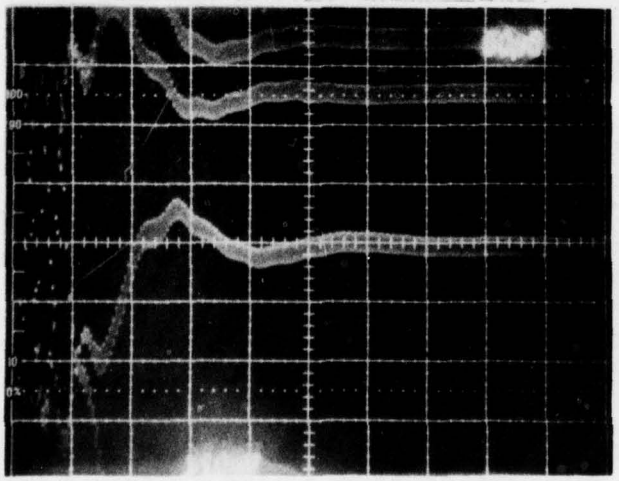
Figure 115. Phase settling of AS/PLL output sinusoid.



187.5 KHz TO LOCK AT 212.5 KHz



201.0 KHz TO LOCK AT 200.0 KHz



212.5 KHz TO LOCK AT 187.5 KHz

Figure 116. Phase settling of filtered triangular staircase AS.

Over the operating bandwidth, the PLL does not function as a narrowband filter as is the usual case, but as a synchronous sampler. Because of this, any deviation from linearity of the sawtooth caused by the PLL circuitry will result in regeneration of spurii amplitudes (a function of the residue value) on the sawtooth as the phase control loop of the PLL forces the sawtooth slope to pass through points defined by a linear sawtooth. This change in slope causes a variation in the time at which the ramp voltage is "dumped", thus resulting in phase modulation of the sawtooth and the output sinusoid.

The above spurii regeneration by the PLL circuitry was verified by the increased spurii amplitude which occurred when the sawtooth was deliberately distorted. Although not discussed in this report, further confirmation of this fact was noted when a triangular waveform was used instead of the sawtooth as the controlled signal of the PLL.

Since the triangular wave contains no even multiples of the fundamental frequency, every other spurious was eliminated while the amplitudes of those remaining where less than the amplitude of their sawtooth counterparts. Based on this, work was done (and is covered in this report) on a triangular waveform AS without the PLL but followed by the same bandpass filter used to filter the sawtooth. The results demonstrated the advantage of a symmetrical waveform since the spectrum obtained was only 10 dB to 20 dB worst than the spectrum of the sawtooth PLL within 250 Hz of the desired output frequency and in most cases only 10 dB at frequencies farther removed.

In the present AS/PLL, most spurii which are not 70 dB below the output occur for output frequencies above 200 kHz (or midband). The spectral purity could be improved 1) if the upper band limit were 200 kHz and the lower limit were 175 kHz rather than the specified 212.5 kHz and 187.5, respectively; or 2) if the clock frequency (f_c) were increased slightly, yet maintaining an output band of 187.5 kHz to 212.5 kHz.

Except for frequencies where a product of the output frequency and the AS clock frequency are within approximately 25 kHz of each other, the design goal of 70 dB spurious was obtained. Random phase noise is at least 100 dB/Hz and is limited by the sawtooth generator and PLL noise rather than by the AS. Settling times were well within the specification limits of 300 μs and were shown to be approximately 75 μs.

Future work on the AS/PLL should include:

- Phase locking of triangular rather than staircase signals.
- Further investigation of triangular wave/bandpass filter combination.

- Investigation of highly linear buffer amplifiers.
- Generation of the linear sawtooth or triangular waveforms by means which do not require buffer amplifiers between the generation circuitry and the phase control and output circuitry.

E. PREDICTED RELIABILITY OF SYNTHESIZER MODULE

1. Introduction

The reliability prediction for the Arithmetic Synthesizer/Phase-Locked Loop is based on a parts count analysis (in terms of failure rate and MTBFs) of the design configuration of the delivered modules.

Part failure rates were derived from MIL-HDBK-217B, dated 20 September 1974, "Reliability Prediction of Electronic Equipment."

The prediction is given for a 50° C part ambient for a benign ground environment, assuming a 50 percent electrical stress level for parts. A 100 percent duty cycle was utilized in obtaining the failure rate and MTBF "Figures of Merit."

The prediction technique employed the simple summation of the failure rates of the total parts complement.

2. Results of Analysis

This latest part count reliability prediction resulted in a predicted use MTBF of 54,116 hours. A summary of the data is as follows:

Part population: 187

Use failure rate: 18.479 $F/10^6$ hours

Use MTBF: 54,116 hours

This data was derived from the reliability analysis as covered by subsequent tables. The underlying ground rules are presented in Table 12. Part failure rates were derived from MIL-HDBK-217B, and the specific factors for each part type are shown in Table 13. Table 13 also presents a failure rate summary by part types.

TABLE 12. GROUND RULES FOR PART FAILURE RATES

1. MIL-HDBK-217B is the source of numerics.

2. Electrical stress on discrete parts is assumed to be 50%. This should generally be conservative.

3. Local part ambient is 20° C above a room ambient temperature of 30° C; a local part ambient of 50° C is assumed.

4. Printed wiring boards and connection failure rates were considered negligile and are not included in this analysis.

5. Connector failure rates were based on the static failure rate (λ_b) alone. The cycling factor (λ_{cyc}) was not considered. Assumed <40 cycles/1000 hours.

6. ICs procured to vendor equivalent of MIL-STD-883, Method 5004, Class B.

7. Inductive Device Insulation Class (max. operating temp.) assumed: MIL-C-15305-B (130° C).

TABLE 13. DERIVATION OF PART FAILURE RATES

Part Type	Quantity	Part Type Use Failure Rate for Benign Ground Environment at 50° C (F/10^6 hours)	Total Part Type Use Failure Rate (F/10^6 hours)
Transistors			
Si, NPN ≤1 W	2	0.0280	0.056
Si, PNP ≤1 W	2	0.0420	0.084
FET	6	0.0570	0.342
Diodes			
Si, ≤1 W	3	0.0060	0.018
Zener	5	0.0200	0.100
Integrated Circuits			
Digital	9	0.1300	1.170
Linear	5	0.2800	1.400
SOS LSI	3	1.3600	4.080
Resistive Components			
Carbon Comp. (RCR—5)	14	<0.0001	0.001
Film (RNC-H-5)	25	<0.0001	0.003
Film (RLR—5)	40	<0.0001	0.004
Variable Cermet (Bourns 3082P)	3	2.7640	8.292
Capacitors			
Mica (DM)	12	0.0080	0.096
Ceramic (CKR—R)	31	0.0010	0.031
Tantalum, Solid	15	0.1300	1.950
Inductive Components			
Tunable	6	0.0108	0.065
Ferrite Beads	2	0.0500	0.100
Connectors			
Printed Circuit (8 active pins)	1	0.056	0.056
Coaxial	2	0.0950	0.190
Miscellaneous			
Digital-Analog Converter	1	0.4410	0.441
TOTAL:	187		18.479

Appendix A

PLL BANDPASS FILTER AND LOWPASS FILTER

The output bandpass filter (BPF) is a five-section open-circuit-to-terminated Tchebycheff configuration. Analysis of this filter was done on a time-share computer program (MATCH). The results are given in Tables 14 and 15.

TABLE 14. BPF IN-BAND ATTENUATION AND PHASE DELAY

FREQUENCY (KILOHZ)	L:S21 (DECIBELS)	D:S21 (MILLISEC)
180.00	8.6739	.035219
185.00	6.0834	.045089
190.00	7.1775	.031020
195.00	7.7945	.025721
200.00	6.0707	.038346
205.00	6.8588	.035983
210.00	8.1483	.037529
215.00	11.663	.053073
220.00	24.257	.014250

The output lowpass filter (LPF) was added to suppress the harmonics of f_o generated within the output emitter-follower. Characteristics of this balanced impedance Cauer filter (03 15 35) are given in Tables 16 and 17.

TABLE 15. BPF ATTENUATION

FREQUENCY (KILOHZ)	L:S21 (DECIBELS)
100.00	102.89
110.00	95.288
120.00	87.358
130.00	78.856
140.00	69.435
150.00	58.532
160.00	45.010
170.00	25.371
180.00	8.6709
190.00	7.1775
200.00	6.0707
210.00	8.1483
220.00	24.257
230.00	40.076
240.00	50.563
250.00	58.571
260.00	65.080
270.00	70.569
280.00	75.313
290.00	79.489
300.00	83.217
310.00	86.584
320.00	89.653
330.00	92.472
340.00	95.078
350.00	97.502
360.00	99.768
370.00	101.89
380.00	103.90
390.00	105.79
400.00	107.59

TABLE 16. LPF IN-BAND ATTENUATION (L) AND PHASE DELAY (D)

FREQUENCY (KILOHZ)	L:S21 (DECIBELS)	D:S21 (MILLISEC)
180.00	.13273	.0013538
185.00	.12951	.0014033
190.00	.12889	.0014569
195.00	.13195	.0015148
200.00	.14021	.0015769
205.00	.15463	.0016431
210.00	.17766	.0017131
215.00	.21124	.0017862
220.00	.25783	.0018616

TABLE 17. LP ATTENUATION

FREQUENCY (KILOHZ)	L:S21 (DECIBELS)
100.00	.16402
110.00	.17246
120.00	.17740
130.00	.17827
140.00	.17478
150.00	.16710
160.00	.15508
170.00	.14354
180.00	.13273
190.00	.12889
200.00	.14001
210.00	.17766
220.00	.25783
230.00	.43145
240.00	.63392
250.00	.98316
260.00	1.4757
270.00	2.1313
280.00	2.9590
290.00	3.9550
300.00	5.1056
310.00	6.3924
320.00	7.7973
330.00	9.3075
340.00	10.917
350.00	12.631
360.00	14.462
370.00	16.440
380.00	18.612
390.00	21.063
400.00	23.940
410.00	27.551
420.00	32.688
430.00	42.949
440.00	42.202
450.00	34.007
460.00	30.255
470.00	27.926
480.00	26.298
490.00	25.085
500.00	24.145
530.00	22.283
560.00	21.229
590.00	20.590
620.00	20.201
650.00	19.973
680.00	19.854
710.00	19.811
740.00	19.822
770.00	19.873
800.00	19.954

Appendix B

AS/PLL BOARD ALIGNMENT PROCEDURE

Initial frequency word is set to give 200-kHz output. (See algorithm in Appendix C for obtaining decimal to binary conversion on HP35 or HP45 calculator.) Refer to Figure 55 and perform the following steps:

1. Remove Q9 and connect sweep generator to ground and to R81, R83 junction through 1 μF capacitor. Terminate sweep generator between sweep generator and 1 μF capacitor with 50 ohms. Set sweep generator to cover 200 kHz center frequency ±100 kHz (deviation can be adjusted to give suitable display during filter alignment). Terminate J1 output with 50-ohm spectrum analyzer previously adjusted for 200 kHz center frequency (by injection of 200 kHz fixed frequency) and 10 kHz per division (or ±50 kHz display width).

2. Apply power and adjust analyzer bandwidth control and sweep rate (typically 3 kHz and 0.1 s/div) for consistent display shape with video bandwidth of 100 Hz.

3. Tune L1, L2, L3, L4, L5 to obtain passband of at least ±15 kHz centered on 200 kHz. Proper setting of the inductors is obtained when the passband edge drops down on the low frequency side for a decrease in any inductor and drops down on the high side for an increase in any inductor. (This effect appears as a "seesaw" motion of the flat top of the passband curve as the inductors are "rocked" around the proper adjustment point.) Very slight final adjustment should be made to minimize passband ripple.

4. Turn off power; remove sweep generator and replace Q9.

5. Turn on power and check at U11-8 for sampling pulse.

   a. If not present, proceed backwards through the clock pulse circuitry to locate trouble.

   b. If present, check for inverted signal at Q2-3 approximately centered around 0 V.

6. With sampling pulse present, check U7-14 for staircase waveform.

   a. If not present, check for inputs U7-1 through U7-10. All should be present and must switch between <0.7 to >2.4 V. If inputs not present, check "carry out" of U2 to U4 (pin 20) for presence of a signal and, if necessary, proceed backwards to U16B input and output (both sides of jumper 6) for clock pulse.

7. If staircase is present, check J2 for presence of sawtooth.

   a. If not present, note whether level is at ground or some negative voltage. Turn R45 CCW if level at ground to see if sawtooth appears (CW if level is below ground).

   b. If sawtooth does not appear, check U14-7. This level should be at ground if J2 level is more negative than U13-6 (set by R45 and should be approximately -1.6 V), and >2.4 V if more positive than U13-6. Replace U14 if above conditions do not exist. If R45 cannot set U13-6 to -1.6 V, replace U13 first. If problem still persists, check Q4 and Q5. If still no sawtooth signal at J2, ground Q2-1 and vary R68 to set Q8-2 to approximately -9 V. If -9 V cannot be obtained, check circuitry from Q2 to Q8; if -9 V can be obtained, check to see if sawtooth can be obtained by adjusting R45. (Position of R78 is not critical; however, it should not be at an extreme resistance setting.) If sawtooth still not obtained, more detailed circuitry testing is necessary which is out-of-scope of this procedure. If sawtooth obtained, remove ground from U2-1 and proceed.

   c. If sawtooth obtained, adjust R45 to obtain "locked" sawtooth of 5-μs period. "Locked" condition can be detected by sudden shift in period of sawtooth when "lock" is obtained.

8. Vary R68 to "unlocked" sawtooth condition in both CW and CCW direction. Set R68 to approximately midrange of the CW and CCW position of unlock.

9. Using spectrum analyzer, adjust R45 for minimum spurii on display (or for no tilt to line drawn through tips of sawtooth peaks at Q2-2).

10. Program frequency for 187.5 kHz and 212.5 kHz. Alternately, shift these frequencies into module and check that "lock" is maintained. Adjust R68 as necessary to maintain lock.

11. Set frequency to 212.5 kHz and adjust R45, R68 and R78 for minimum spurii level or low side of 212.5 kHz (approximately 20 kHz and 40 kHz removed). Recheck lock range of 10. above. Repeat step 4.

12. Check output sine-wave level for 0.3 V rms over output band (187.5 kHz to 212.5 kHz). Level may vary 4 dB over band.

Appendix C

DETERMINATION OF AS/PLL INPUT WORD SIZE USING HP-35 or HP-45

To determine the input word sequence required to produce a desired output frequency for the AS/PLL, the technique detailed in Table 18 may be used on an HP-35 or HP-45 calculator.

TABLE 18. DETERMINATION OF INPUT WORD SEQUENCE

Line	Data	Key Operations	Display	Remarks
1	Clock Frequency	Enter	Clock Frequency	Enters clock frequency.
2	Accumulator Size	Enter	Accumulator Size	Enter number of accumulator stages
3	2	X^Y ÷	Size of LSB Change	
4	Desired Output Frequency	(↻) ÷	Decimal value of input step size (NF)	
5		EEX		Start round off to integer.
6	9	+ EEX		
7	9	-		NF rounded to integer.
8	0.5	STO	0.5	
9	2	÷	$\frac{NF}{2}$	a) If decimal part of $\frac{NF}{2}$ = 0, LSB = 0. b) If decimal part of $\frac{NF}{2}$ = 0.5, LSB = 1.
10	a) If 9a; 2	÷	NF/4	
	b) If 9b;	RCL -	NF/2	NF/2 = rounded to integer.
	2	÷	NF/4	
11	If NF/4 decimal part = 0, enter 0 in next higher LSB. If NF/4 decimal part = 0.5 enter 1 in next higher LSB.			

Note: Repeat operations of 10 and 11 until division by 2 = 0.

The following calculations illustrate the use of this technique:

Given:

Clock frequency = 1×10^6 MHz

Accumulator size = 24 stages

Desired output frequency = 187, 500 Hz

Line	Display after required key operations	
1	1EXP06	
2	24	
3	0.0596046449	
4	3145727.989	
5	1 EXP00	
6	1 EXP00	
7	3145728	
8	0.5	
9a	1572864	LSB = 0
10a	786432	next LSB = 0
10a	Repeat until:	
10a	3	$2^{19} = 0$
10a	1.5	$2^{20} = 1$
	1.0	
10a	0.5	$2^{21} = 1$
	0	
10a	0	STOP

∴ Step size = 001100000000000000000000 (base 2)

To check for actual output frequency:

Step size = 3145728 (base 10)

$$f_o = \frac{\text{(clock frequency) (step size)}}{2^X}$$

where X = number of accumulator stages.

$$\text{Therefore } f_o = \frac{(1 \times 10^6)\ (3145728)}{2^{24}} = 187,500 \text{ Hz.}$$

END
6-77